FPGA 2032 Roadmap : A Personal Perspective

Learn from Yesterday

2012

1992

Blackberry

Courtesy : Don McMillan

Learn from Yesterday

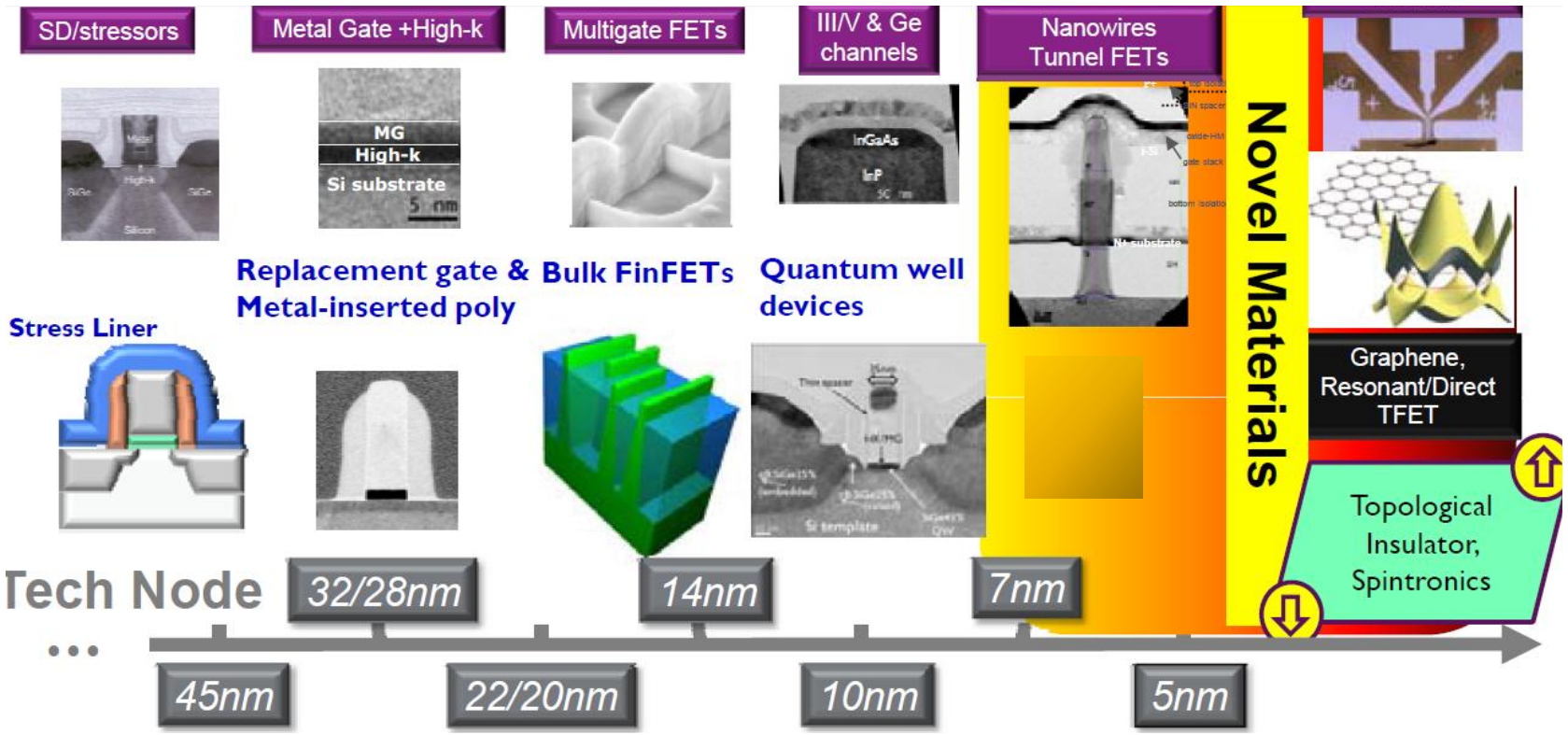
2012

1972

Cell Phone

Courtesy : Don McMillan

Silicon Roadmap



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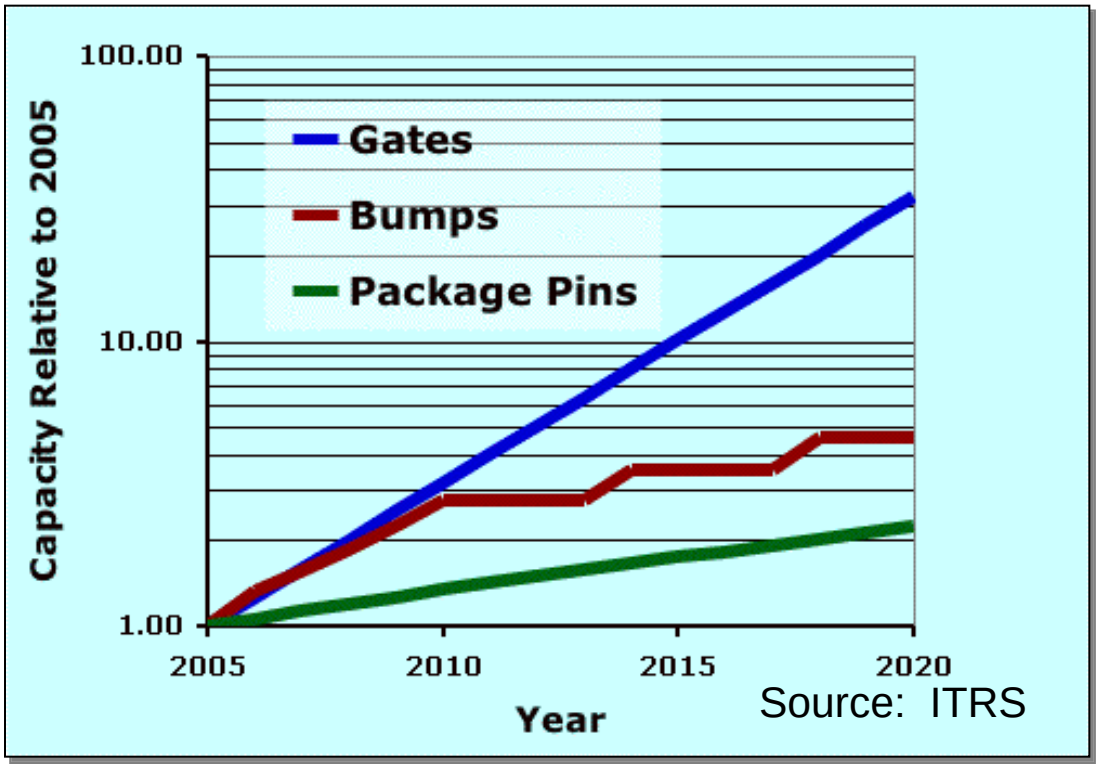
Interconnect

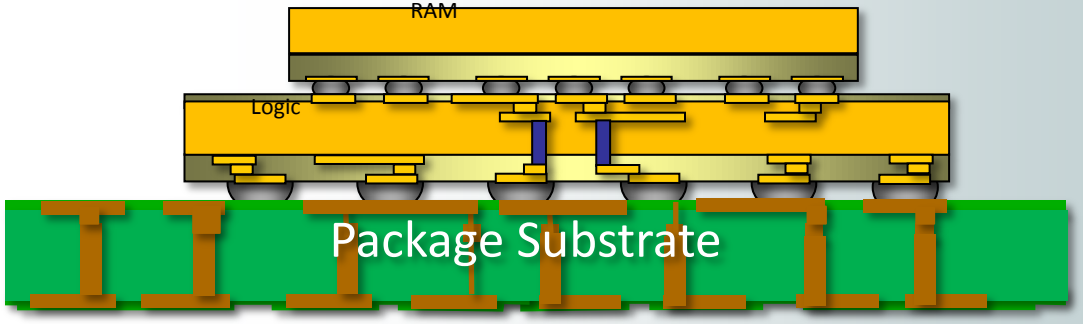
- Growing gap between number of logic gates and I/O
- Technology scaling favors logic density



15x drop in I/O-to-logic ratio by 2020

What Does 2.5D and 3D Buy Us?

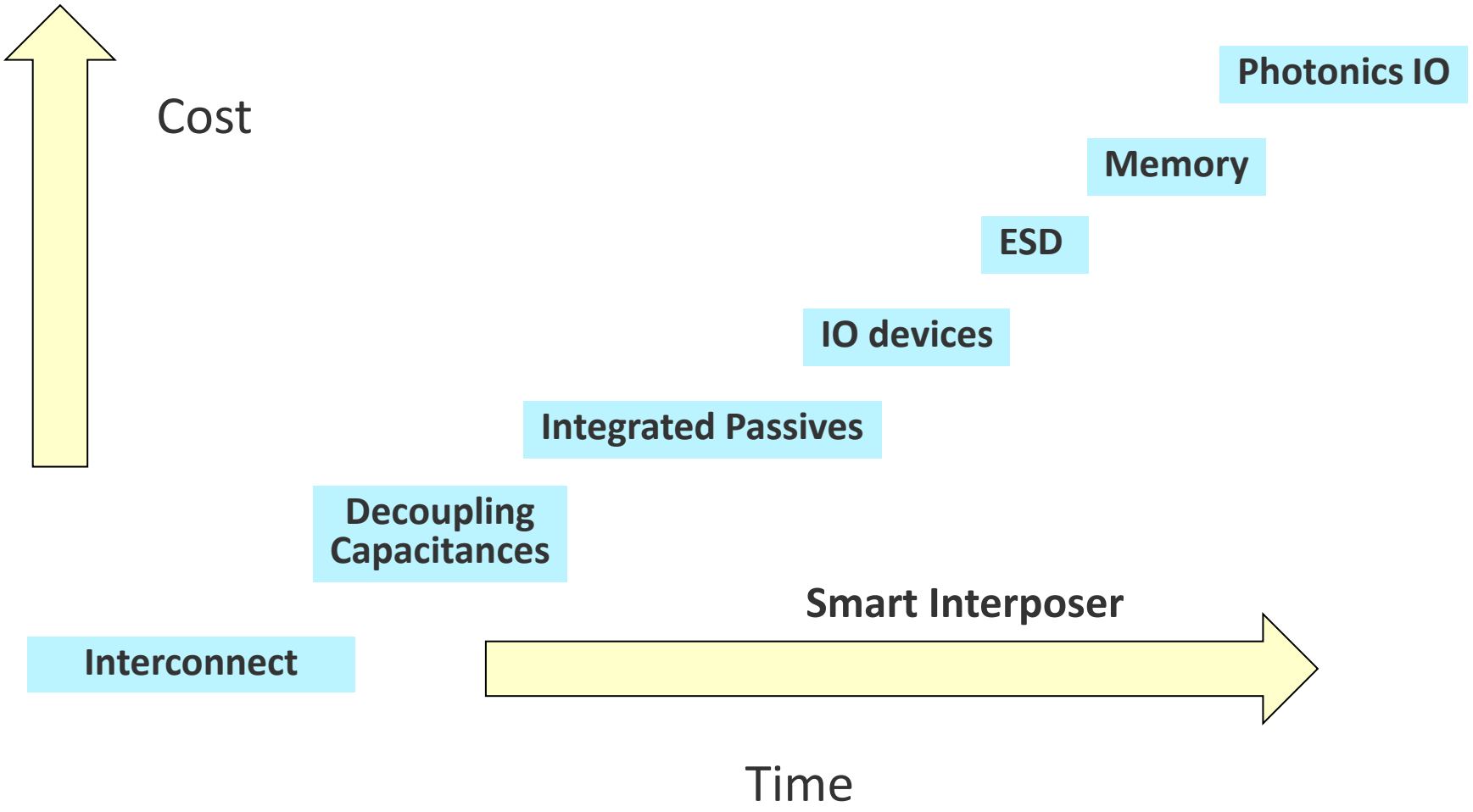
- Connectivity
- Capacity
- Crossovers



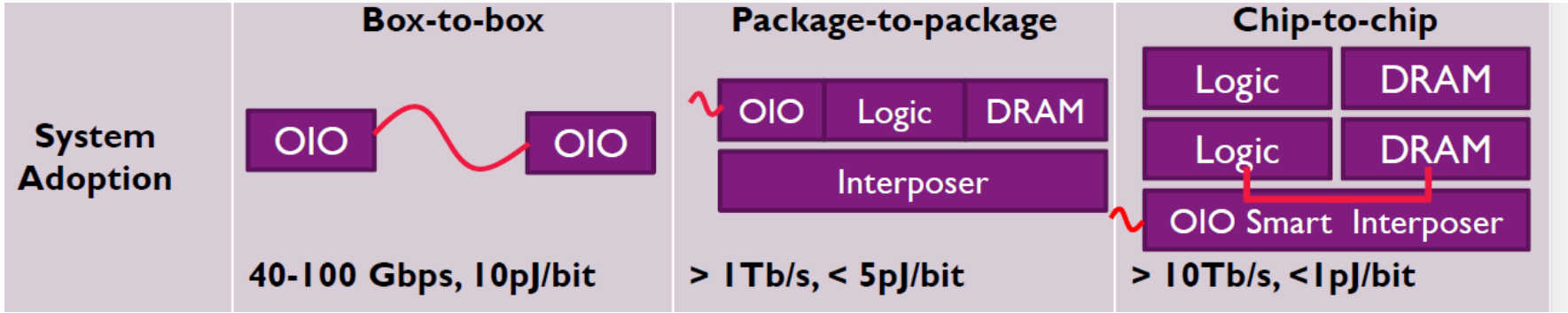
3D versus 2.5D

	3D	2.5D
Design Flow	New Co-Design	Evolutionary
Device impact	Stress	None
Cost	High	65nm Interposer
Thermal	Challenging	Evolutionary
Testing	New Methods	Evolutionary
Reliability	Challenging	Evolutionary

2.5D and 3D Interconnect

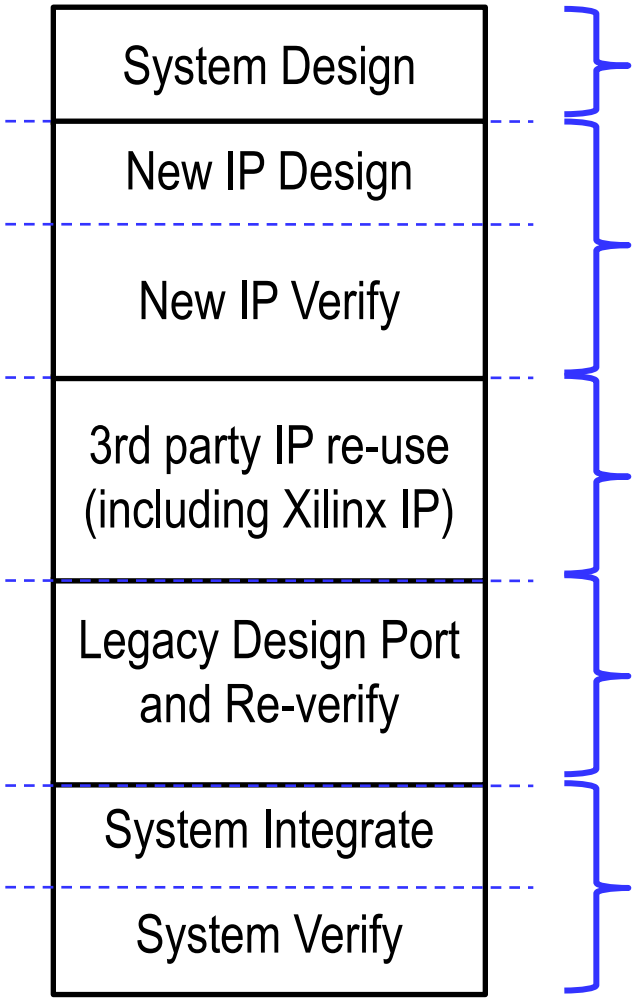


Optical Interconnect



2012 2015 2020

ASIC Use Model



System design (function to microarchitecture)		
Per 5kLC core	1	man-week

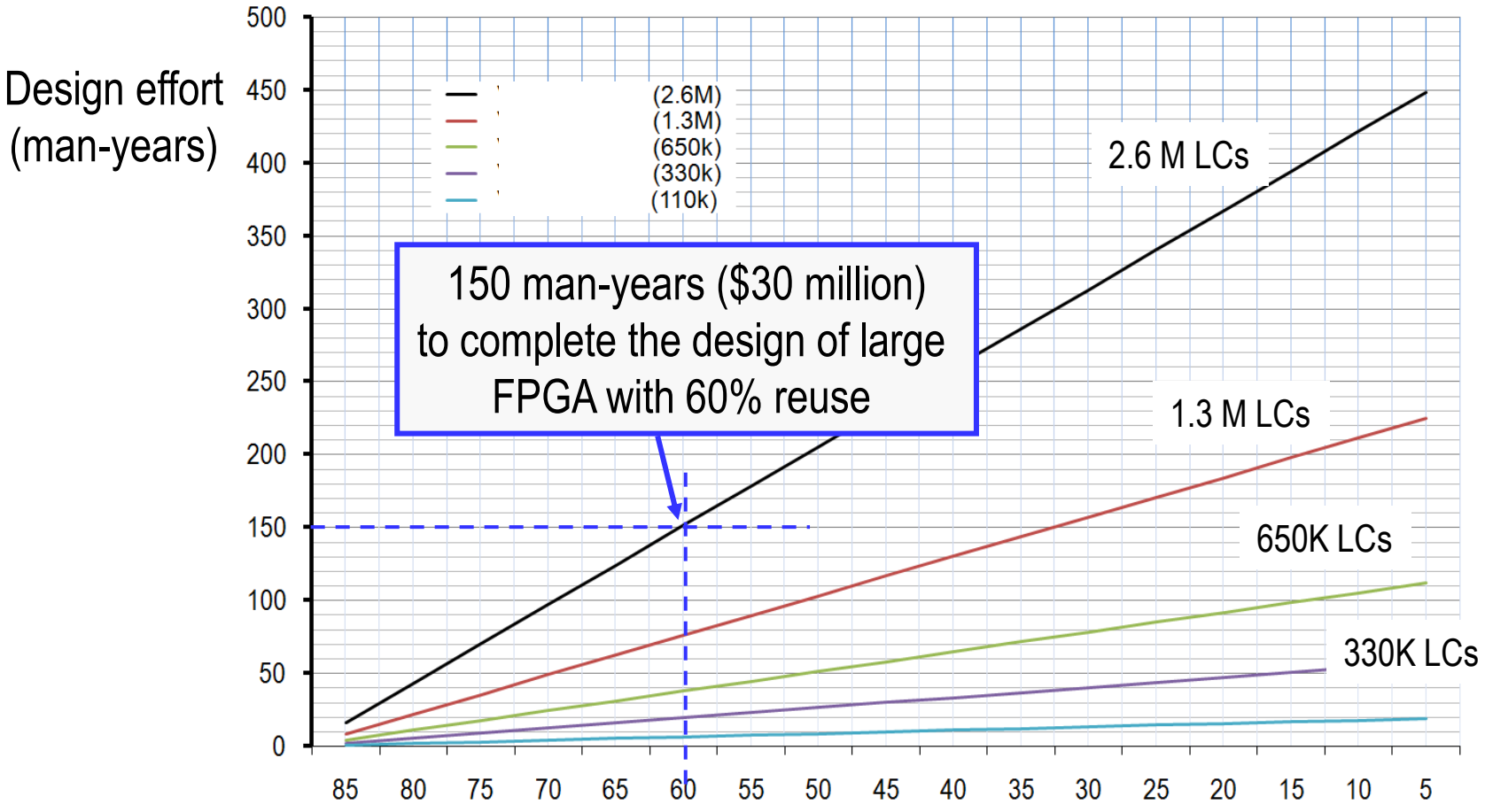
New core creation (5kLC cores)		
Design	15	man-weeks
Verification	30	man-weeks
Total	45	man-weeks

3rd-party Core Re-use (per core)		
Assessment	7.5	man-weeks
Verification	15	man-weeks
Total	22.5	man-weeks

Legacy core port to new device (per core)		
Port	0.5	man-weeks
Re-verify	1	man-weeks
Total	1.5	man-weeks

Final system integration & verification (per core)		
Core integration	0.5	man-weeks
System verification	1	man-weeks
Total	1.5	man-weeks

Model of FPGA HW customer design effort



Note: maximum 85% device utilization is assumed

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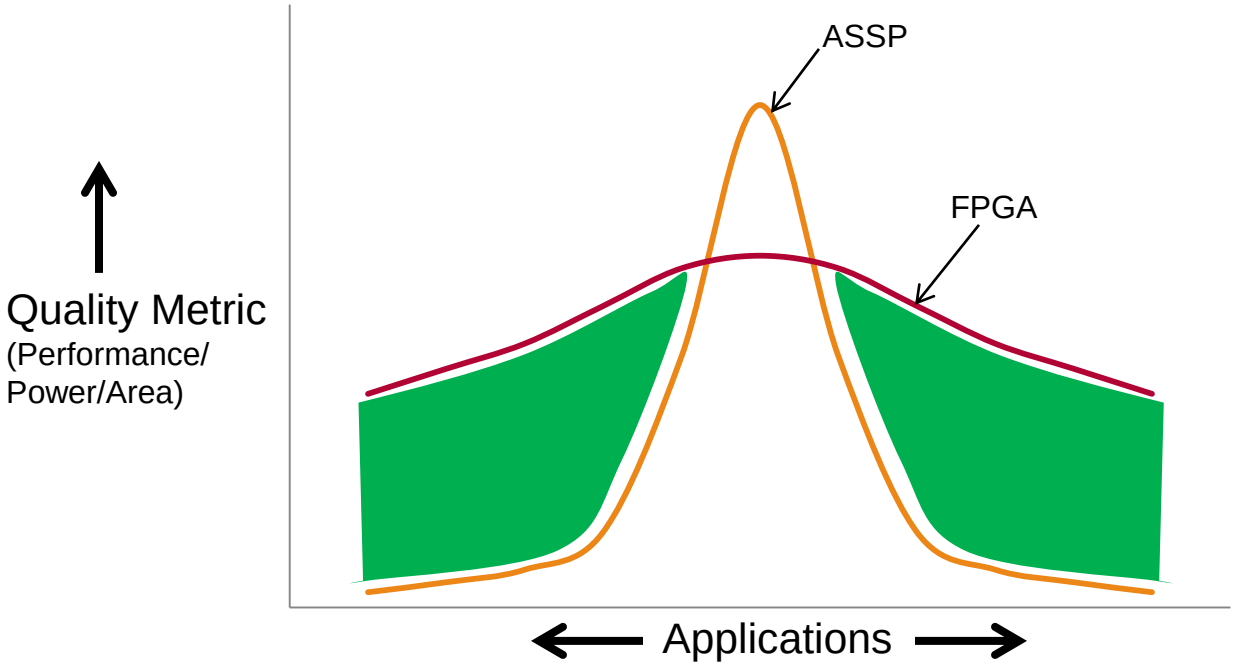
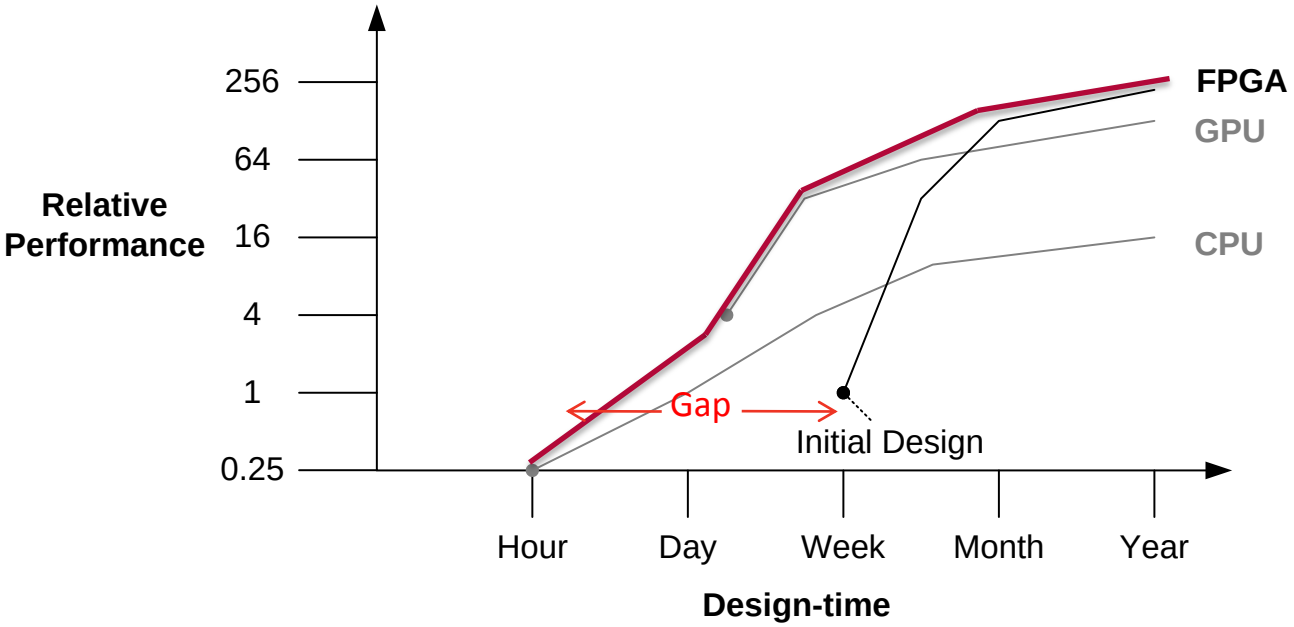
SW Use Model : FPGA and Multi-core ASSP



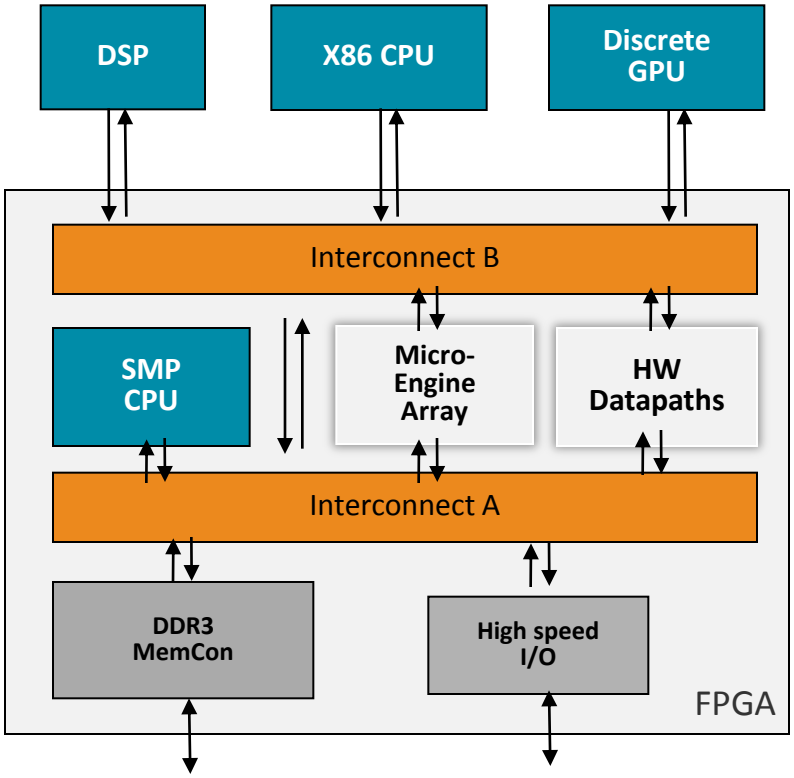
Need for Design Tools



Courtesy : David Thomas

The Programmable Processing Platform

A heterogeneous multicore



- **Application processors**
  - Hard core and soft core
  - External and embedded
  - Caches and large memory space
  - Unified shared memory
  - Full OS support
- **Streaming micro-engines**
  - Configurable (soft) vector cores
  - Tiny memory footprint
  - Many, distributed, memories
  - Compute kernels, no OS
- **Fixed function datapaths**
  - C to Gates generated
  - HDL coded
  - Library IP component

FPGAs provide a rich set of mapping options for complex algorithms and communication patterns

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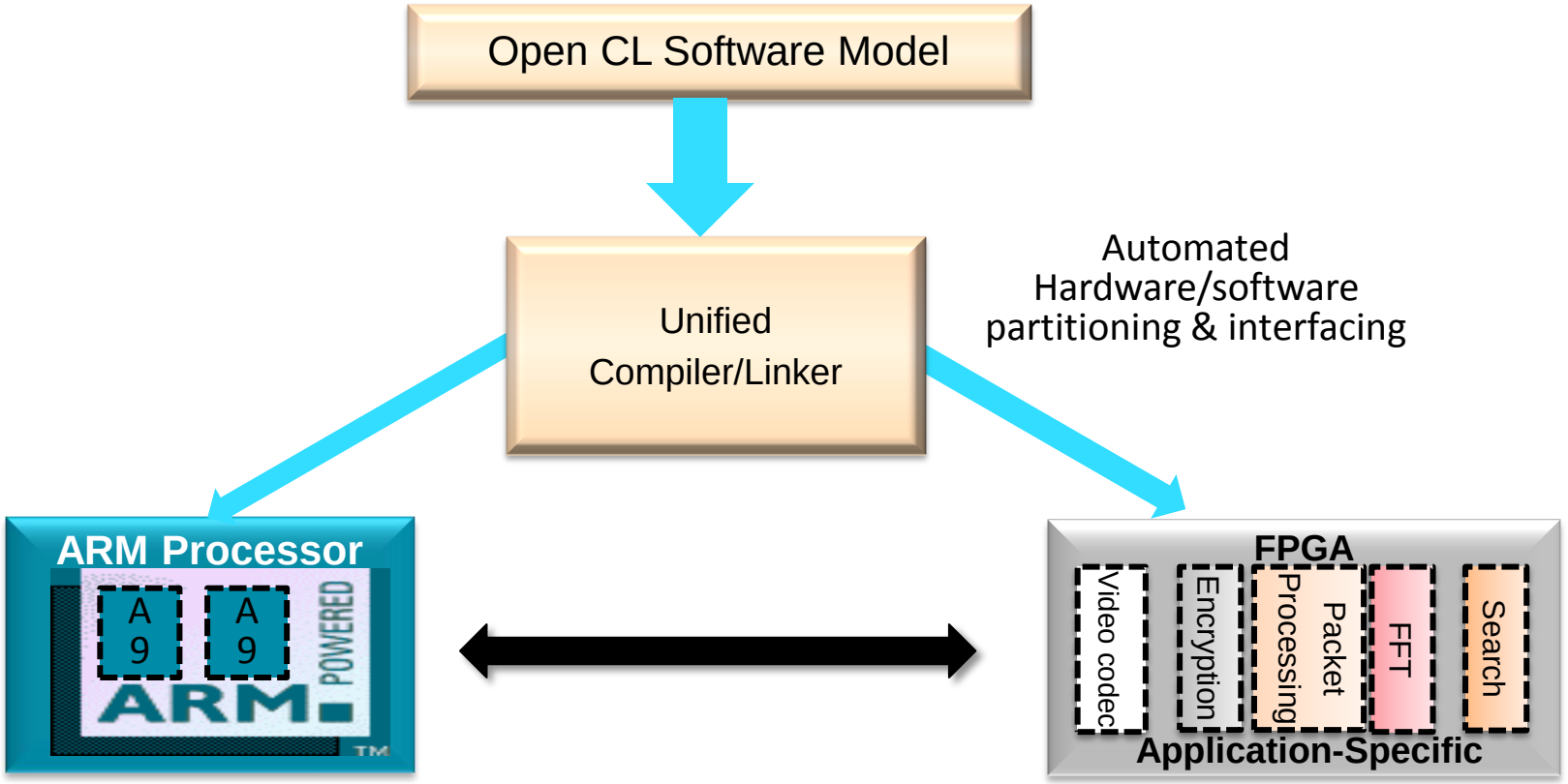
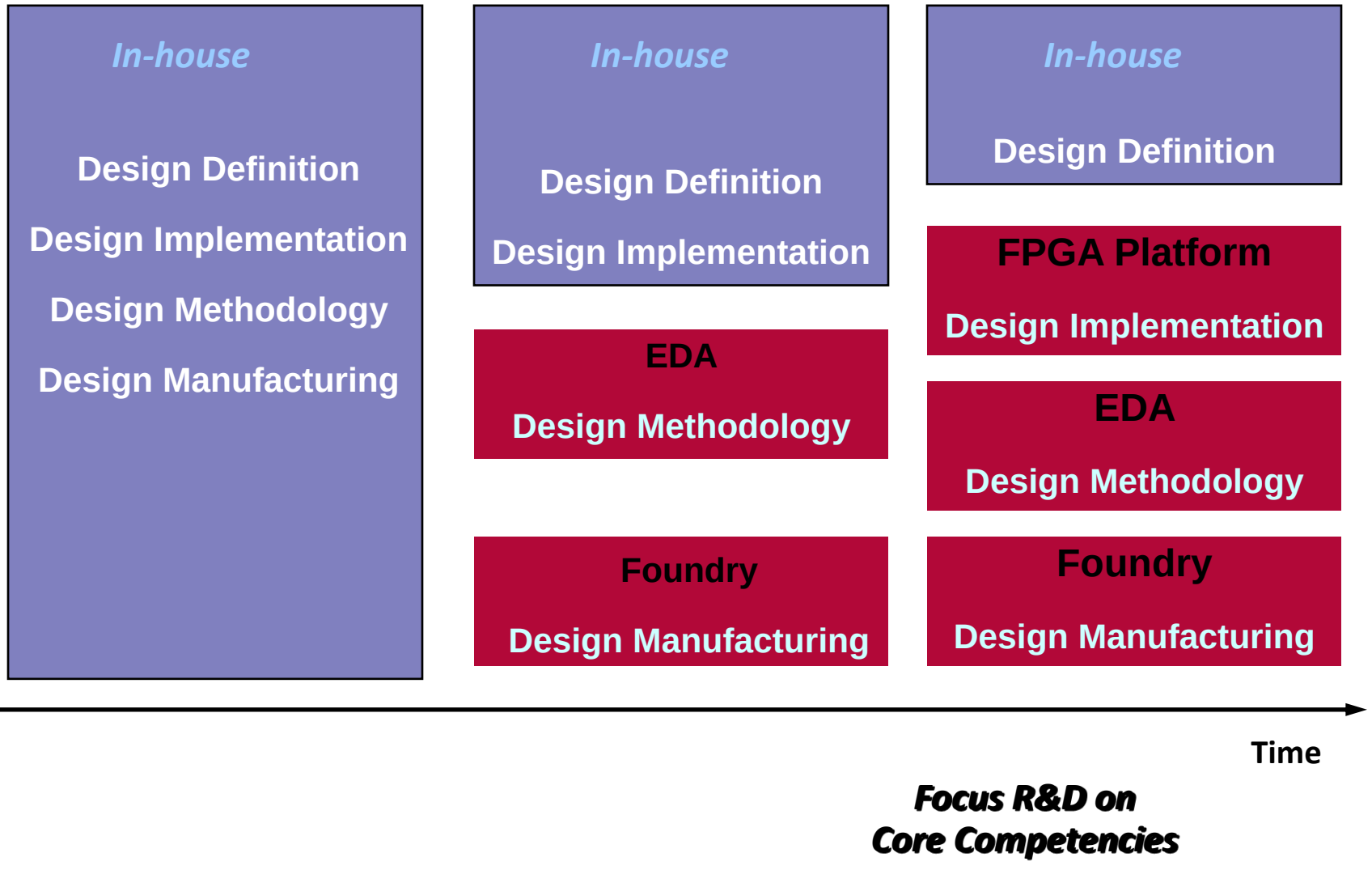
Parallel Programming



Application Level Programming of Heterogeneous Multi-core

The Design Stack



Focus R&D on Core Competencies

Conclusions : 2032 FPGA

- Silicon Technology Roadmap continues

  Challenges : Variability, Fault tolerance, Power limited, Cost

- 2.5 D and 3 D essential

  Opportunity : Connectivity, Capacity, Heterogeneity

- HW Design Methods handle complexity

  - Re-Use

  - Modular Design Flow/Architecture + 10 min 1M LC P&R

  - 33% utilization : dark silicon/fault tolerance

- Software Use Model

  - Parallel programming

  - Heterogeneous Multi-core

  - Solve Timing Closure

The Singularity

- 10^{10} Transistors = 10^{10} Neurons
- Parallel Architecture
- Synapse : 10^{3} denser interconnect
- Fault tolerant
- Asynchronous
- Adaptable
- Content Addressable Memory
- 10^{7} more energy efficient