FPGAs in 2032: Challenges and Opportunities in the next 20 years

Convergence of Programmable Solutions

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Tempting Topic Not Discussed Here

- Predictions from 1992 about 2012
 - Accurate ones
 - Hilarious ones
 - Probably more accurate than now predicting 2032.

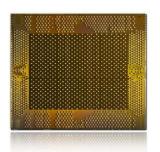
1990s 2010s

Glue Logic



Flex 6000 3µ process

Heterogeneous Capabilities



Stratix I 130nm process

High Integration/ Bandwidth



40nm process

Hardened Subsystems



28nm process

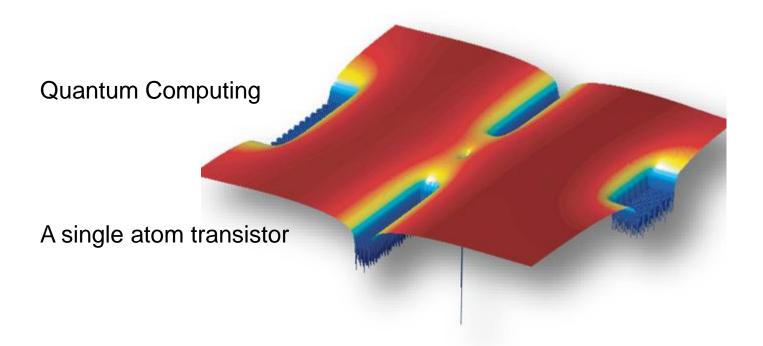
Cortex-A9 MPCore



SoC FPGA 28nm process



Tempting Topic Not Discussed Here



A controllable transistor engineered from a single phosphorus atom has been developed by researchers at the University of New South Wales, Purdue University and the University of Melbourne. The atom, shown here in the center of an image from a computer model, sits in a channel in a silicon crystal. (Credit: Purdue University)



Tempting Topic Not Discussed Here

DNA computing

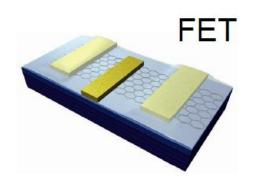
 Scientists at IBM are experimenting with using DNA molecules as a way to create tiny circuits that could form the basis of smaller, more powerful computer chips.

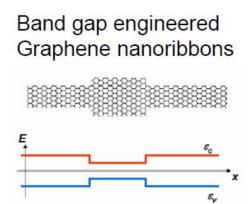




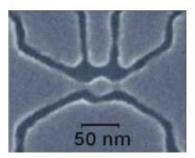
Tempting Topics Not Discussed Here

Conventional Devices



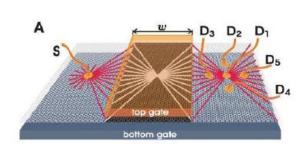


Graphene quantum dot



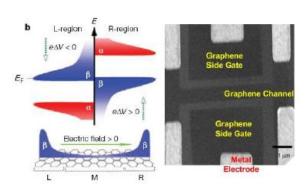
(Manchester group)

Nonconventional Devices



Graphene Veselago lense

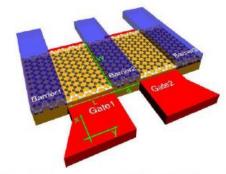
Cheianov et al. Science (07)



Graphene Spintronics

Son et al. Nature (07)

P. Kim – Columbia U.



Graphene pseudospintronics

Trauzettel et al. Nature Phys. (07)



Tempting Topics Not Discussed Here

- Wonderful applications of technology in 2032
 - 6 billion connected people
 - 100 billion connected devices
 - Internet of Things
 - Wearable electronics
 - Genome informatics and personalized medicine
 - Intelligent robots and machines
 - Singularity
 - Many others...



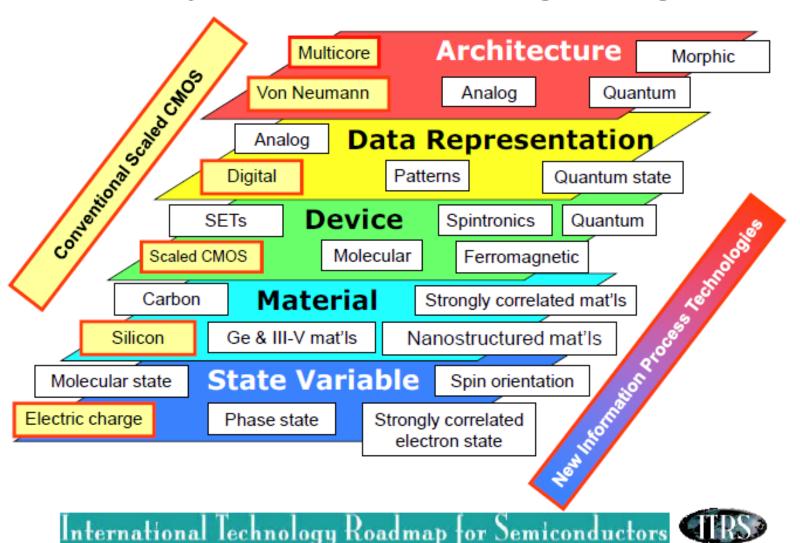
Topics Discussed Today

- Convergence of programmable platforms
- A need for programming models, languages and compilers for converged programmable platforms
- Summary



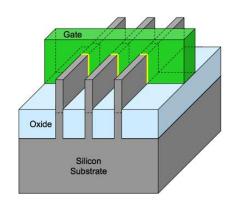
ITRS Roadmap Ends In 2026

A Taxonomy for Nano Information Processing Technologies

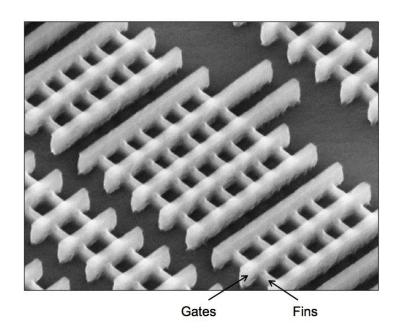




Intel 22nm FinFET Announced May 2011



			A COMMON OF STREET		
Process Name	P1266	P1268	P1270	P1272	P1274
Lithography	45 nm	32 nm	22 nm	14 nm	10 nm
1st Production	2007	2009	2011	2013	2015



Claimed benefits relative to 32nm:

- 18% faster at 1.0V, 37% faster at 0.7V
- 50% lower power at same performance
- 2-3% higher cost than planar process



"More Moore" Projections

Year	2012	2014	2017	2020	2023	2026	2029	2032
Node	20nm	14nm	10nm	7nm	5nm	3.5nm	2.5nm	1.8nm
# FETs per die (B)	8	14	28	56	113	222	453	887
M1 1/2 pitch (nm)	32	24	16.9	11.9	8.4	6	4.2	3
Lgate (nm)	22	18	14	10.6	8.1	5.9	4.2	3

^{*} Normalized to 20nm

Sources: ITRS 2010, ITRS 2011, Altera projections beyond 2026



2032 Process Technology Extrapolation

- "More Moore" scaling produces:
 - ~1 Trillion transistors per die, >100X of 20nm technology
 - 250X increase in throughput compared to 20nm
 - Minimum features of ~13X silicon atomic spacing
 - Faster transistors, but much slower interconnect
- Many significant challenges exist
 - New materials and device structures are necessary
 - Long term options: Tunnel FET, nano wires, graphene, non-CMOS devices
- Slower scaling combined with 3D is an attractive alternative
- More Than Moore can achieve same transistor count as More Moore



IMEC 3D System Integration Program

Logic IDM









FABLESS

OLLALCONNO!



















3D PROGRAM









MATERIAL SUPPLIERS



Hitachi Chemical





EDA

SYNOPSYS°

cādence°











EQUIPMENT SUPPLIERS



TOKYO ELECTRON







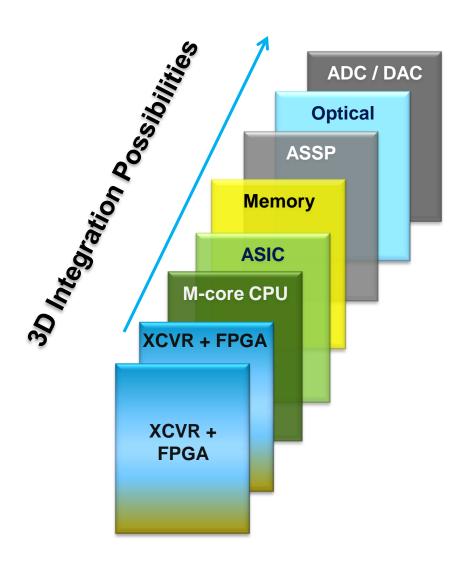






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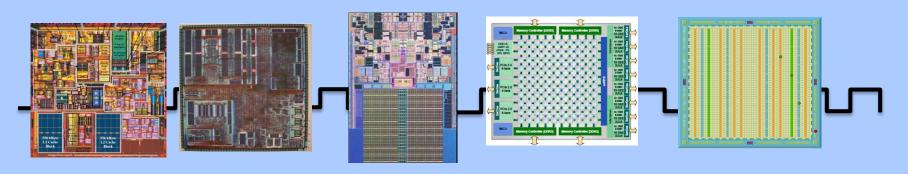
3D Integration Technology Opportunities





Programmable Platforms in 2012

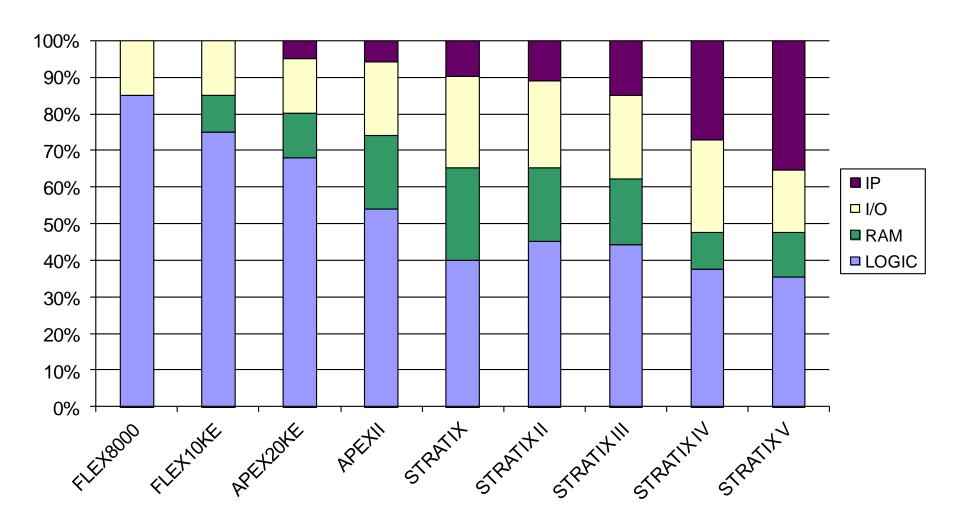
Moore's law has enabled a range high density programmable platforms



CPUs	DSPs	Multi-Cores	Many-Core Arrays	FPGAs
Single Cores	5	Multi-Cores Coarse-Grained CPUs and DSPs	Coarse-Grained Massively Parallel Processor Arrays	Fine-Grained Massively Parallel Heterogeneous Arrays



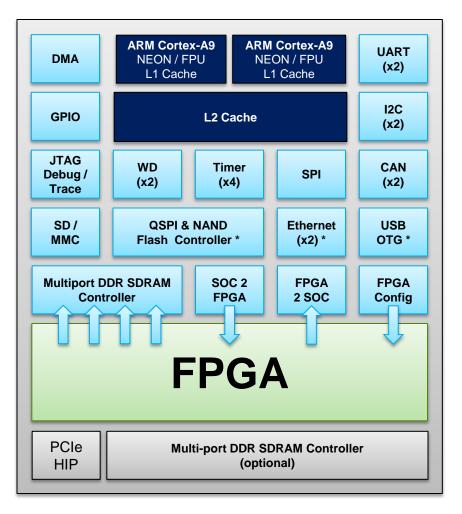
Augmenting Fine-Grained Fabric with Coarse-Grained Programmable Functions in FPGAs





Emerging SoC FPGAs

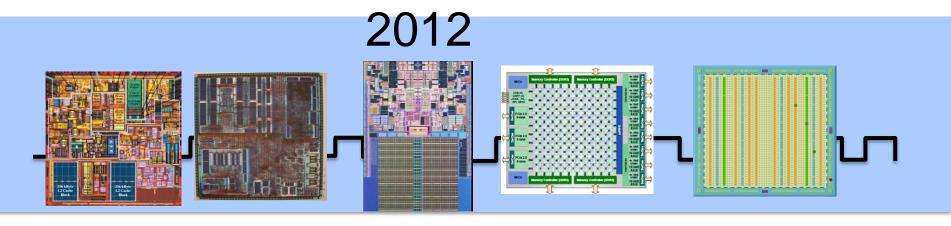
- Processor
 - Dual ARM Cortex-A9
- SDRAM Controller, Peripherals
- Other Hard IP
 - Serial protocols, memory interfaces
- FPGA programmable fabric
 - Multiple density options
- Programming model: C/C++ for ARM
 - Common operating systems
 - APIs for hardware accelerators developed in HDL (Verilog, VHDL, System Verilog), or C/C++ by using high-level-synthesis
 - OpenCL



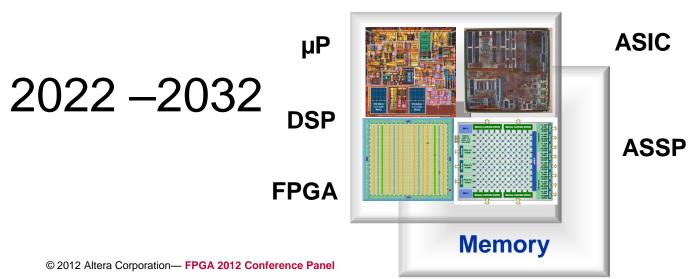
* Integrated DMA logic



Programmable Convergence in 2022-2032



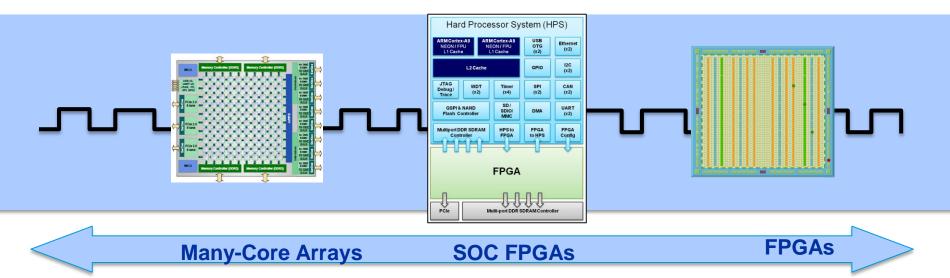
 From 2022 to 2032 all SoCs will be programmable, a combination of today's architectures





Emerging Parallel Programming Models

- Parallel programming is still evolving for many-cores
- OpenCL emerging for many-cores, FPGAs and SOC FPGAs



- CUDA, OpenCL for GPUs,
- Versions of C, C++ and bare-metal programming for many-cores
- OpenCL parallel programming for FPGAs and SOC FPGAs
- C/C++ for ARM with OpenCL for implementing and managing hardware accelerators

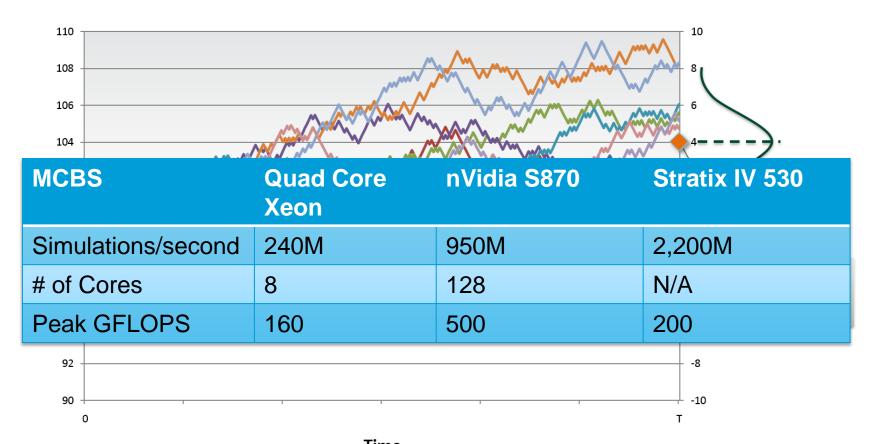


OpenCL Compiler for FPGAs

Host Program

```
main()
  kernel void
sum( global const float *a,
global const float *b,
global float *answer)
                                                                                 Load
                                                                  Load
                                                                         Load
                                           Load
                                                  Load
                                                          Load
int xid = get_global_id(0);
answer[xid] = a[xid] + b[xid];
                                                                                             PCle
int xid = get_global_id(0);
answer[xid] = a[xid] + b[xid];
                                                                             Store
                                              Store
                                                              Store
                                                                                 Load
                                           Load
                                                                          Load
                                                  Load
                                                          Load
                                                                  Load
                                                                                             DDR*
                                                                             Store
                                              Store
                                                              Store
```

Finance: Equity Derivative Pricing



Monte Carlo simulation of all possible paths for the underlying equity value



Summary

- Key directions to 2022 and 2032
 - Convergence of programmable platforms
 - Heterogeneous architectures
 - Programming models and compilers for the converged programmable platforms



