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FPGAs in 2032:

Challenges and Opportunities in the next 20 years

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Learn from history: FPGA ’92 to now

Workshop Report: FPGA ‘92

ACM / SIGDA / ITRC First International Workshop on

Field-Programmable Gate Arrays

Berkeley, CA, USA

February 16-18, 1992

Jonathan Rose

University of Toronto

- Architectures
- CAD Tools
- Emulation
- Applications

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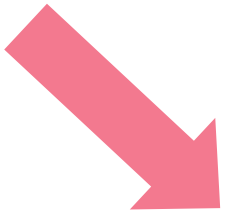
FPGA '92 → '12: Architecture & CAD

Using Architectural and CAD Interactions to Improve FPGA Routing Architectures
B. Tseng, J. Rose, S. Brown
University of Toronto



Much higher **COMPLEXITY**

Higher level of **ABSTRACTION**

The VTR Project: Architecture and CAD for FPGAs from Verilog to Routing
Jonathan Rose, Jason Luu, Jason Anderson and Opal Densmore, University of Toronto
Andrew Somerville and Kenneth B. Kent, University of New Brunswick
Chi Wai Yu, City University of Hong Kong
Jeffrey Goeders, University of British Columbia
Peter Jamieson, University of Miami, Ohio, USA

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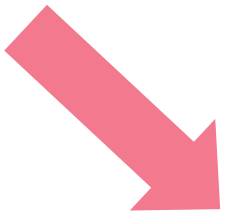
FPGA ’92 → ’12: Automation Tools

Graph-Based FPGA Technology Mapping for Delay Optimization
J. Cong, A. Kahng, K. C. Chen,
P. Trajmar
UCLA



Higher level of **ABSTRACTION**

Optimizing SDRAM Bandwidth for Custom FPGA Loop Accelerators
Samuel Bayliss and George Anthony Constantinides, Imperial College, London

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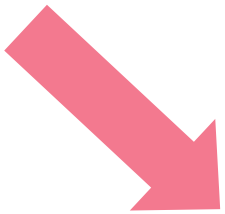
FPGA '92 → '12: Emulation/Prototyping

BORG: A Reconfigurable Prototyping Board Using Field-Programmable Gate Arrays
P. K. Chan, M. Schlag, M. Martin
University of California



Much higher **COMPLEXITY**

A Cycle-Accurate, Cycle-Reproducible Multi-FPGA System for Accelerating Multi-Core Processor Simulation
Sameh Asaad, Ralph Bellofatto, Bernard Brezzo, Chuck Haymes, Mohit Kapur, Benjamin Parker, Thomas Roewer, Proshanta Saha, Todd Takken and Jose Tierno, IBM

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FPGA '92 → '12: Applications

FIR Filters with the Xilinx FPGA
Les Mintzer
Momentum Data Systems

Much higher **COMPLEXITY**

Completely **NEW APPLICATION**

Speedy FPGA-Based Packet Classifiers with Low On-Chip Memory Requirements
Chih-Hsun Chou and Nian-Feng Tzeng, University of Louisiana, USA
Fong Pong, Broadcom Corporation

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My reflections '92 to '12

1. Progress in 20 years – not as dramatic as I expected
   - Still using similar LUT structures, asking similar questions
2. Unexciting but necessary
   - Handling complexity will continue to be a problem next 20 years
   - Need to rely even more on automation tools and raised level of abstraction
3. FPGAs going from strength to strength
   - Both Xilinx Altera stocks ~$2➔~$40
4. Many attempts for new things, and many failures
   - Many startups on new FPGAs and most died
5. FPGA successful as ASIC replacement, but not in algorithm acceleration in general
   - GPU often can do much better
   - Still win on power

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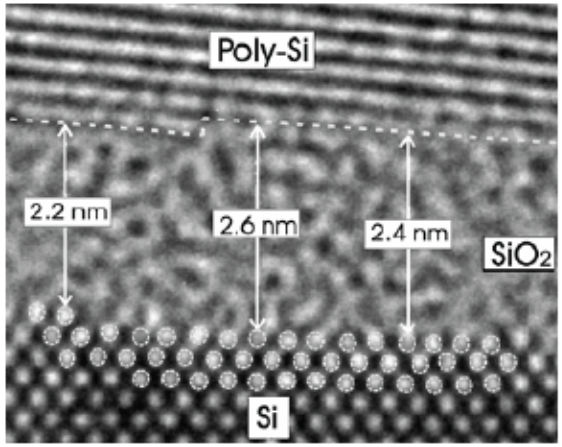
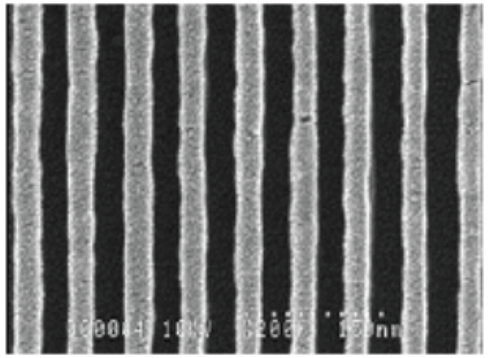
Reliability Related Challenge 1: Process Variability

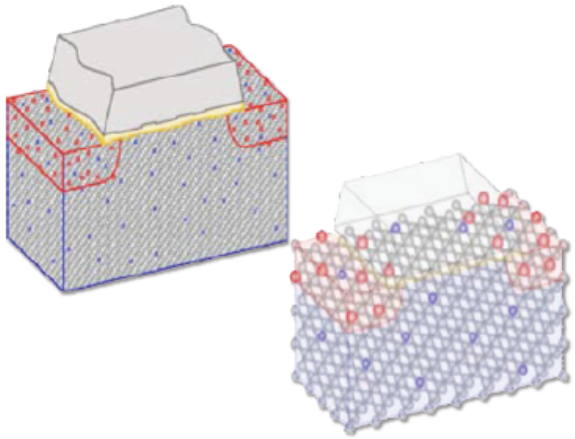
Lithographic tolerances



gate oxide thickness

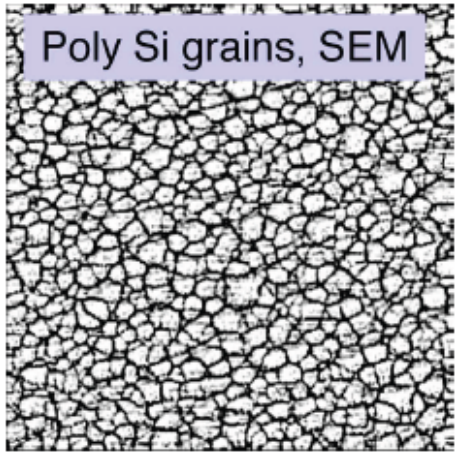


line edge roughness



Random discrete dopants

resist



polysilicon grains

IBM & University of Glasgow

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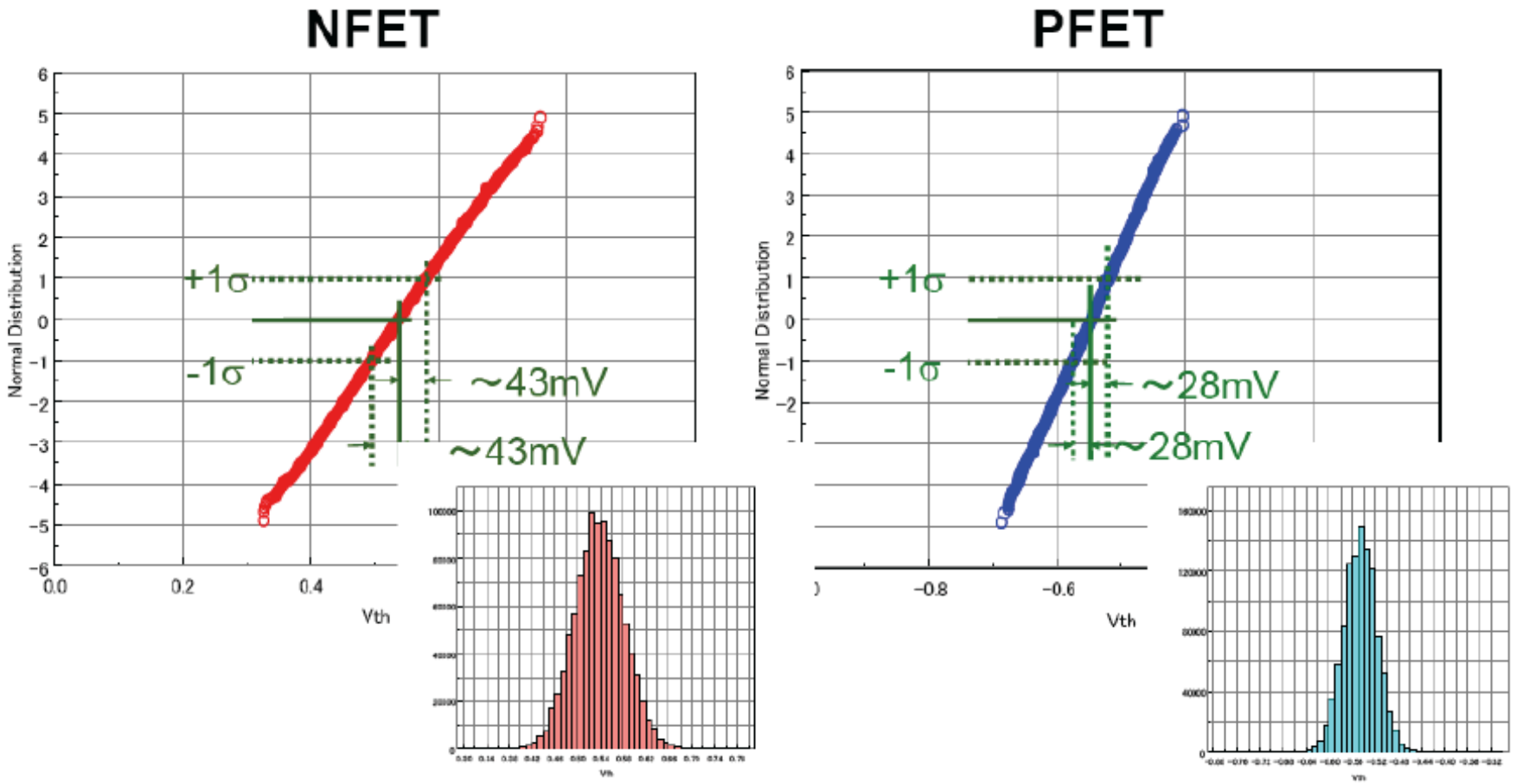
Threshold Variation of 10^6 trans. in 65nm



1. Normal distribution up to ±5σ.
2. NFET has larger variations than PFET.

T. Tsunomura et al., VLSI Symposium, p. 156, 2008.

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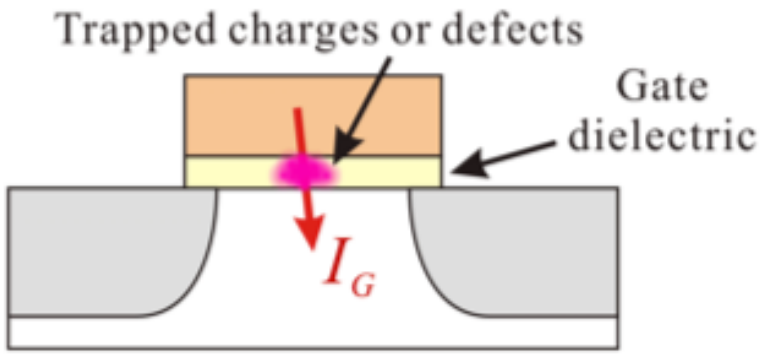
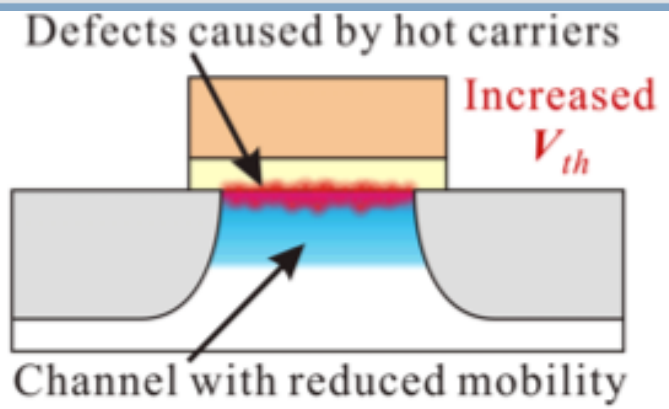
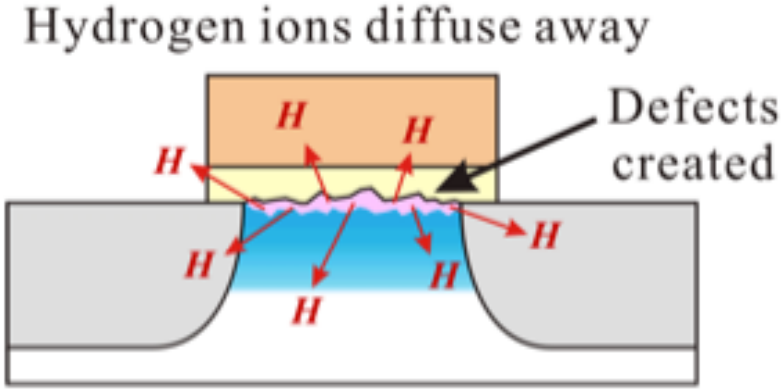
Reliability Related Challenge 2:
Degradations mechanisms



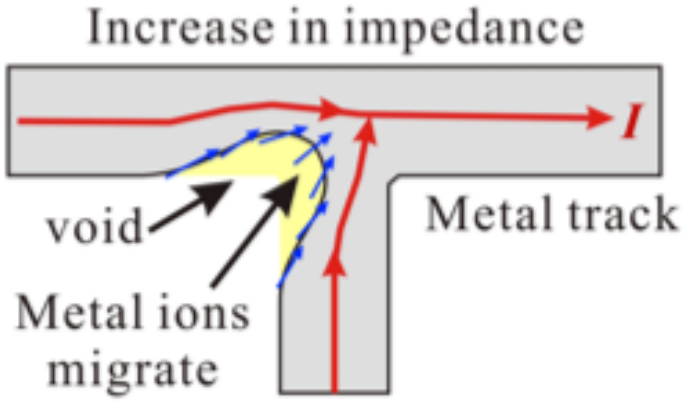
Negative-bias temperature instability (NBTI)



Hot carrier injection (HCI)



Time-dependent dielectric breakdown (TDDB)



Electromigration

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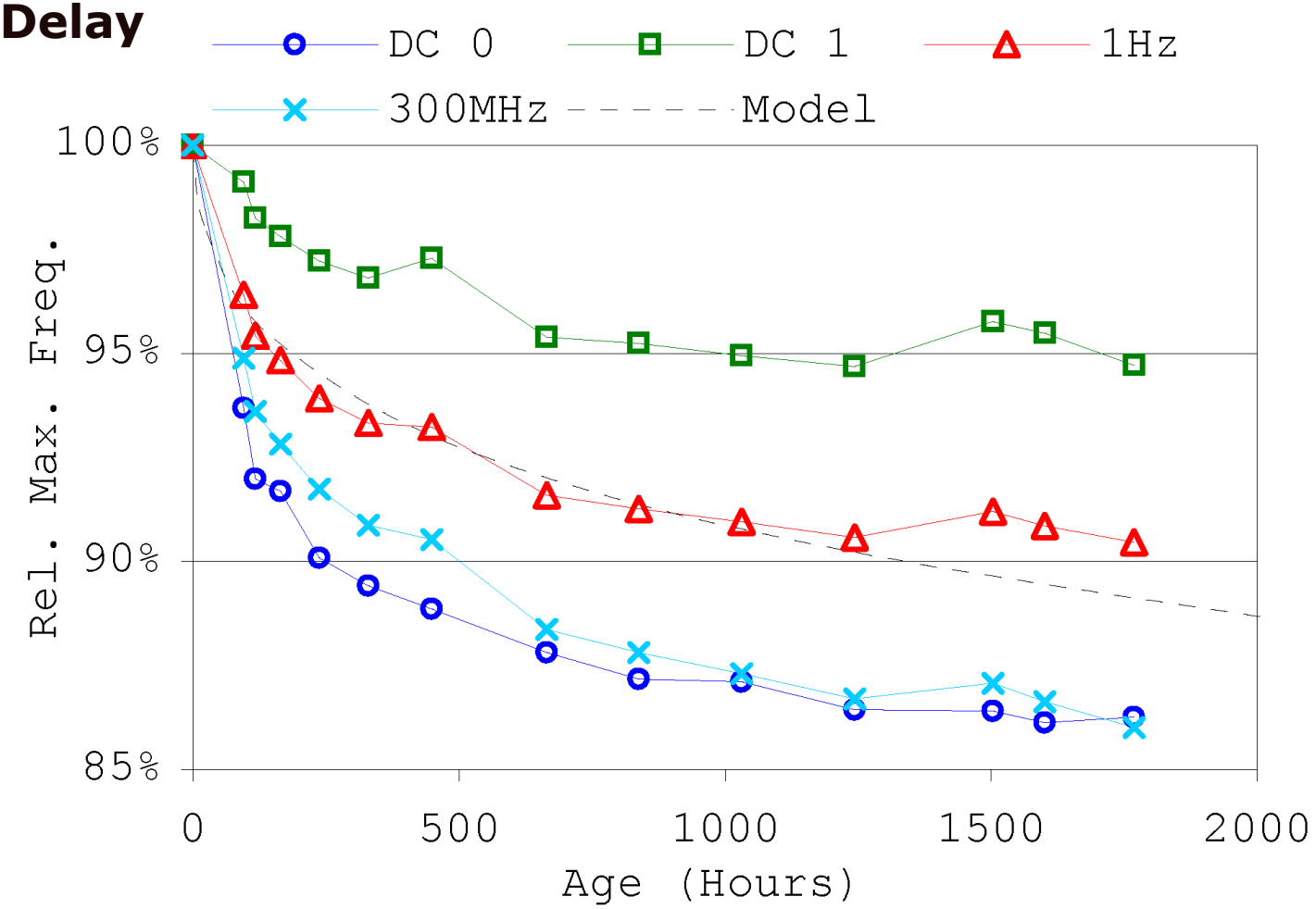
Wear-out effect: Experiment

LUT Delay



E. Stott, J Wong, P. Sedcole and P.Y.K. Cheung "Degradation in FPGAs: measurement and modelling", in FPGA 2010.

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Reliability Related Challenge 3:
Manufacturing Yield

- According to ITRS 2011, before 2026 (end of the roadmap):

> "… the cost of ensuring each and every one of the transistors in a large integrated circuit to function within specification may become too high to be practical."

- Manufacturing yield could fall to near 0%

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Implication of the Reliability Challenges

- The current paradigm will no longer apply:

~~Making chips is like printing money: every chip (and notes) is identical.~~

- Must treat each chip of the same design differently
- Reconfigurable architecture is PERFECTLY PLACED to tackle the Reliability Challenges

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6 Opportunities due to reconfigurability

1. Device specific tuning
   - Already happening, e.g. delay matching of pins
2. Self-test, characterisation and diagnosis
   - Configure for test, then reconfigure for normal use
   - Measure its leakage and delay on powerup(?)
3. Failure prediction
   - Health-monitoring circuit to track degradations
4. Reconfigure/relocate circuits to handle failures
   - Mitigate yield loss by exploiting redundancy
5. Avoid worst-case design
6. Wear-levelling to mitigate degradations

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6 Predictions for 2032

- Xilinx and Altera will still be around
- Reconfigurability is found on all integrated circuits, not just FPGAs
- All electronic gadgets are connected
- Machine learning is an integral part of all electronic systems
- This conference will still only accept 20-24 papers
- U of T still dominates this conference with at least 25% of full papers