FPGA-2012 Pre-Conference Workshop:

FPGAs in 2032: Challenges and Opportunities

Shep Siegel
Atomic Rules LLC

Agenda

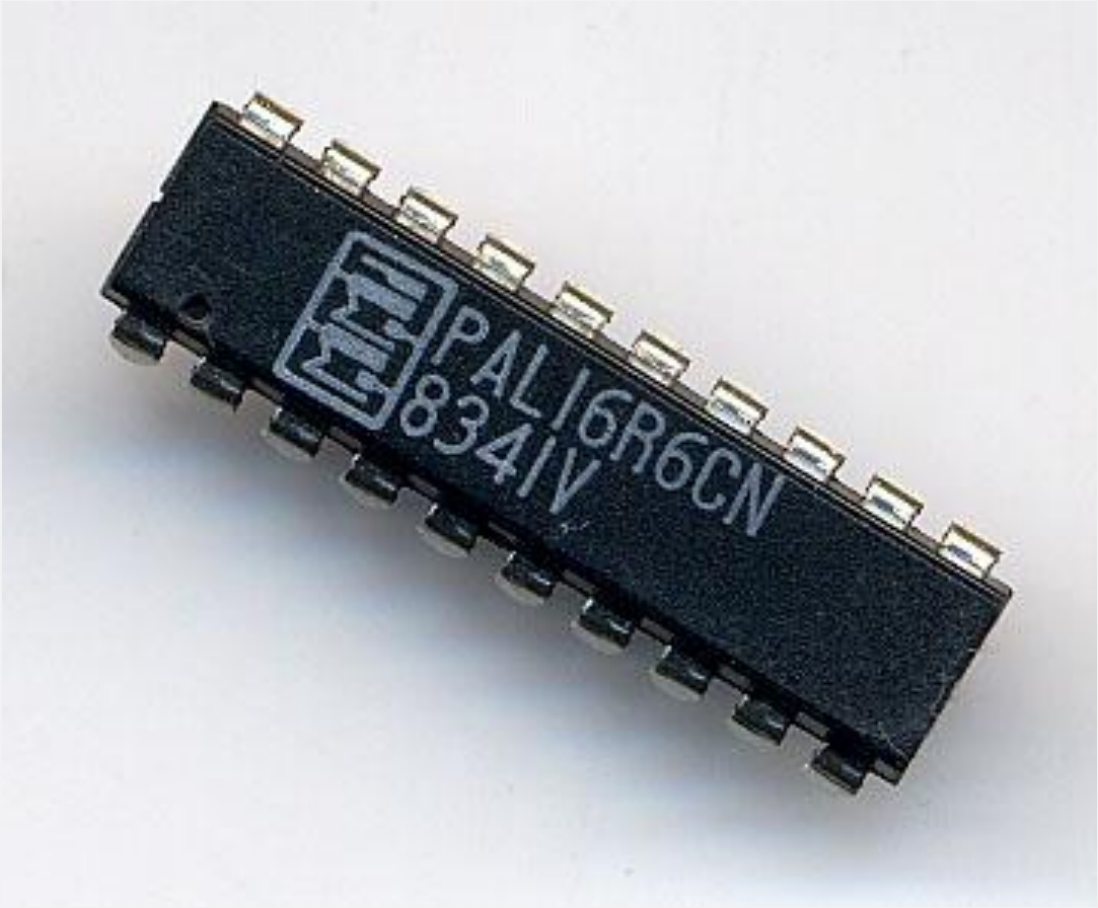
- Pre-History: Our Future from our Past
- How Specialization Changed Us
- Why Research Matters
- Happy Mistakes
- Owning the Problem
- Looking Ahead

Meta Agenda

- Insights from the past
- Problems vexing us now
- Future challenges and opportunities

1978: Birkner, et al @ MMI

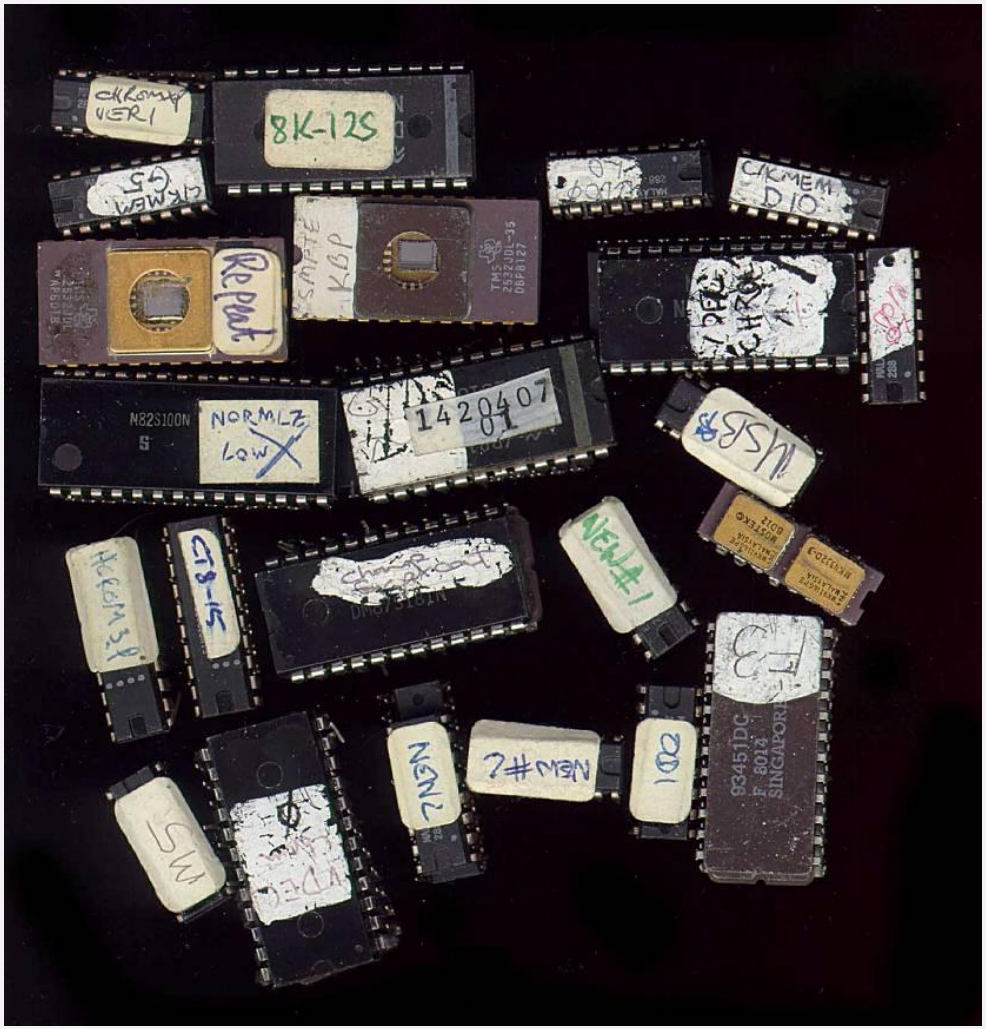
In 1978:
The first FPGA conferences remain 14 years in the future.



Early 1980s: Digital Explosion

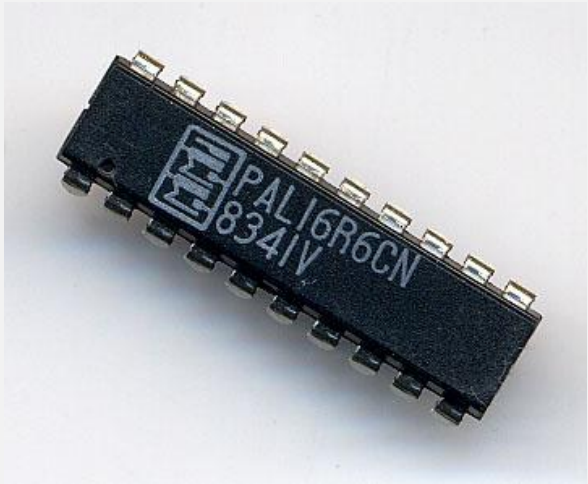
- 16 -> 32 Kb DRAM
- Dense, Switching Power Supplies
- VLSI Multipliers
- Monolithic Video ADCs and DACs
- 100s of 74-series SSI TTL
- CPLDs and ROMs dominate
- Mick and Brick published “Bit-Slice Microprocessor Design”

Early 1980s: ROM and EPROM



~1983: PALs are Mainstream

- Technology FUD displaced by proof points
- Reduced time-to-market
- Enabled postponing logic design decisions
- Less board rework
- Increased density over SSI
- Product-term innovation
  - Karnaugh map challenge



Mid-1980s

- Yes, we know…

- But appreciate the similarities to MMI's child
  - A new cycle of technology FUD
  - Many of the same PAL values, amplified
    - And more: most notably SRAM, not OTP
  - Karnaugh map jockeys become "PIP-bashers"
    - The birth of spatial programming

“These (FPGA) Tools Suck”

- Allegedly heard circa 1985
  - Still seven years to an FPGA conference

- Small engineering teams divided:
  - S/W team: C-codes and OSs
  - H/W team: K-Maps and PIPs
  - System/Application-Domain team: Help!!!

1987: Eli Lilly gets FDA approval for Prozac. Coincidence?

Enough History

- Patterns Repeat
- Local, first-order predictions are often more reliable than a random guess
- Appreciate the Failures as well Successes

Segue: Today

- Hooray for us
- Indisputable Value of FPGA in Industry
- Synergy – whole worth more than the parts
  - Architecture
  - Implementation
  - Time to Solution
  - Specialization
  - Density

Architectural Specialization

- ASIC-Speak “Sea of Gates”
- FPGA-Speak “Sea of *K*-LUTs”

- Functional Heterogeneity matters
  - BRAM, DSP, and SERDES changed FPGA
  - Trimberger FPL 2007 Keynote

Why Research Matters

- Burning need for quantitative measures
- Like-to-Like comparisons are needed
  - Especially between technology choices
- As Engineers, if nothing else, we can measure!
- Helps us decide: “Is this a path worth following?”

Happy Mistakes

- Turn cycles on everything more quickly
- Simulate, Compile, Verify (repeat, automate)
- Incremental tests provide “activation energy” to ratchet process forward

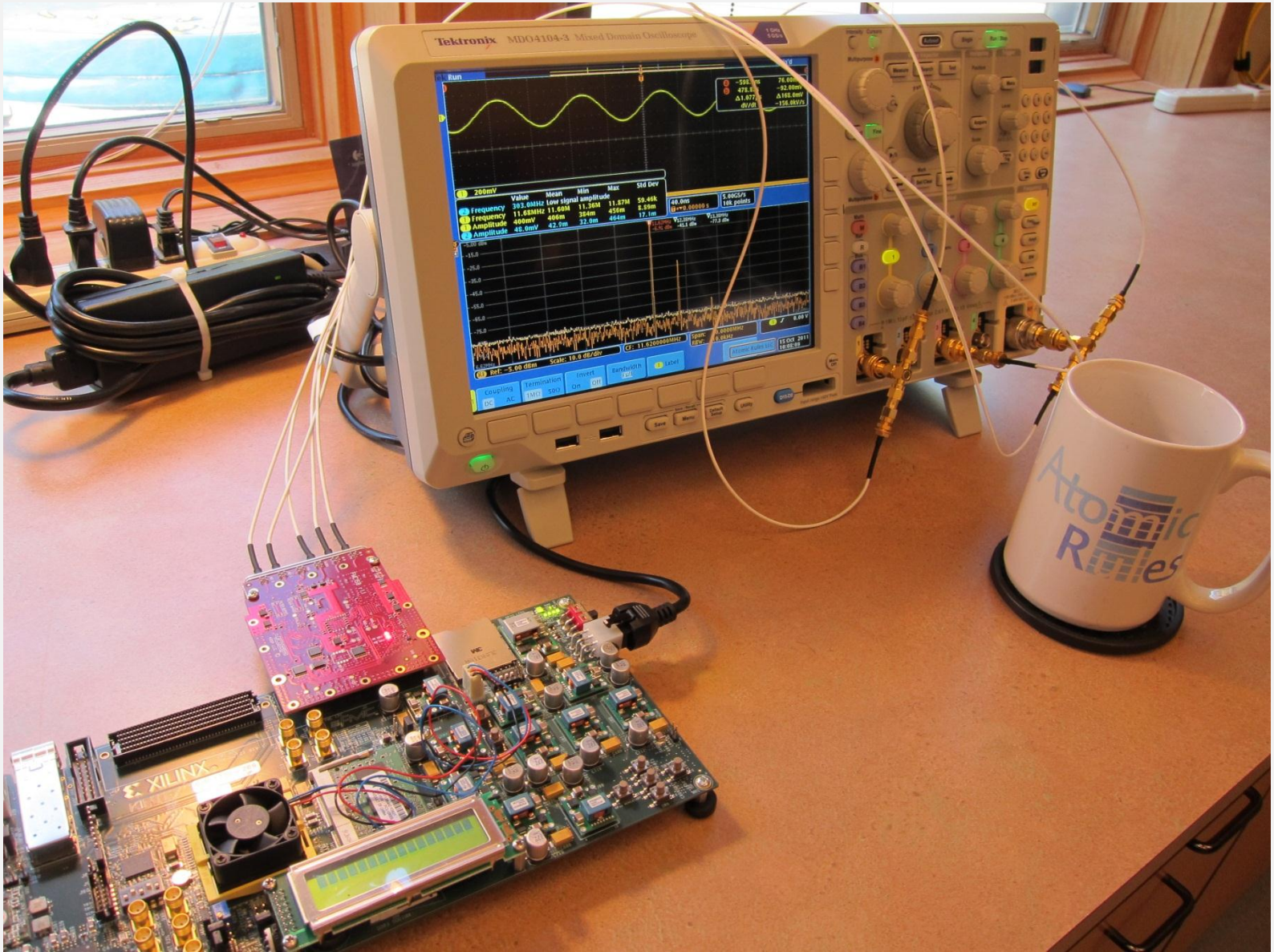
Own the Problem…

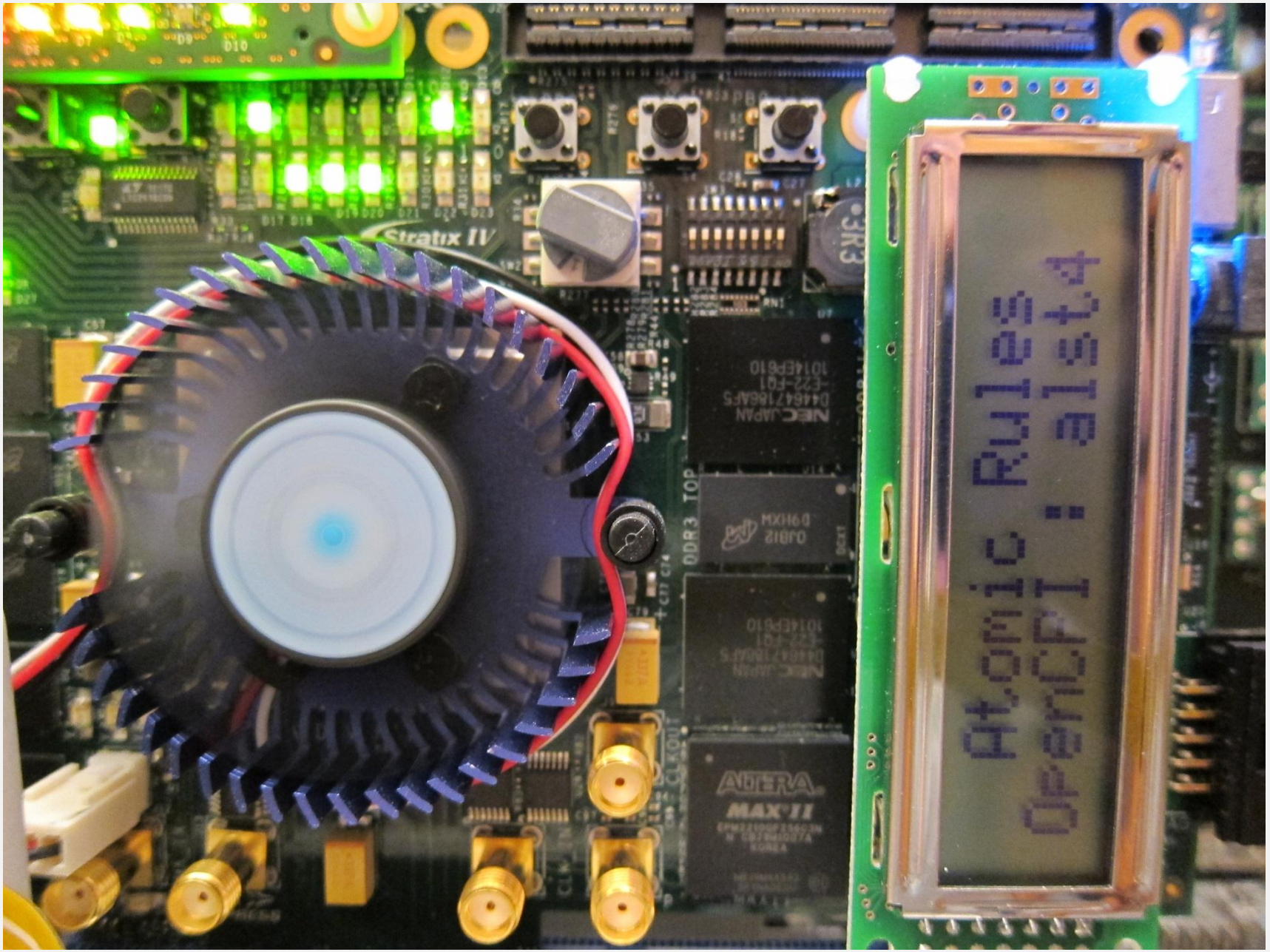
- … Solve it, Check it in!

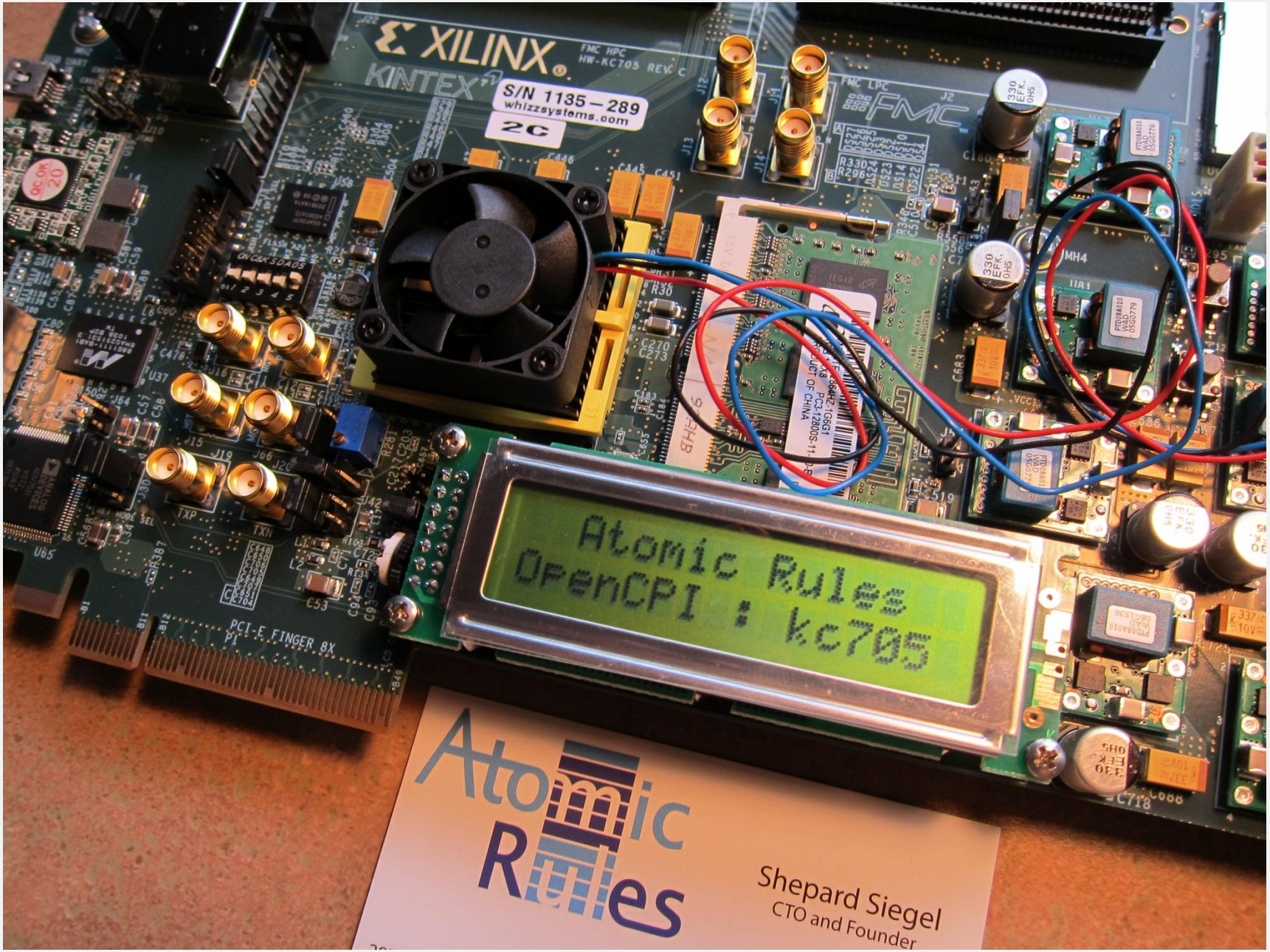
- Agile
- Extension of “Happy Mistakes” process
- Personal “Interface and Implementation”

- As you do this; engage your peers
- Automate your work so it can live on without you

Technology and Business







Enough of Now

- Perform a great number of experiments
- Automate or Die
- Respect business-case distortion fields

Segue: 20 Years On

- We care about the future because we can change it !

- This talk:
  - No device physics, photonics, nano-anything

The Sequential Paradigm

- RTLs are ubiquitous
- Synchronous digital circuits: A solid bet
  - But it is increasingly an “illusion”
- GALS was a start
  - Can we extend GALS in new ways?
- Digital Complex-Concurrency is helped by “Scalable Atomicity”

Correctness: At a Cost

- Maintaining the digital illusion

- Defect concealment
- How will that work, or be practical?

- Already die- and chip- variations…
- What's beyond Si-Moore?

Communication vs. Compute

- Communication historically 2nd class
  - Throughput easy: Wider and Faster
- No longer the case
  - Patterson 2004 “Why Latency Lags Bandwidth”
- Communication challenges outstrip Computational challenges

Complexity

- Almost all complexity reductions help
- $O(N^2)$ problems to 2N
- $O(N^3)$ problems to 3N
- Universe of P and NP problems out there
- Keep chipping away, no matter how small or specialized
  - Projections, Eigenvectors, Basis Functions

The Trouble with Matter

- The 2.5 D physical stacking is wonderful
- 3D will be great some day too
- 3D is not a panacea
- But 3D and speed-of-light set upper bound

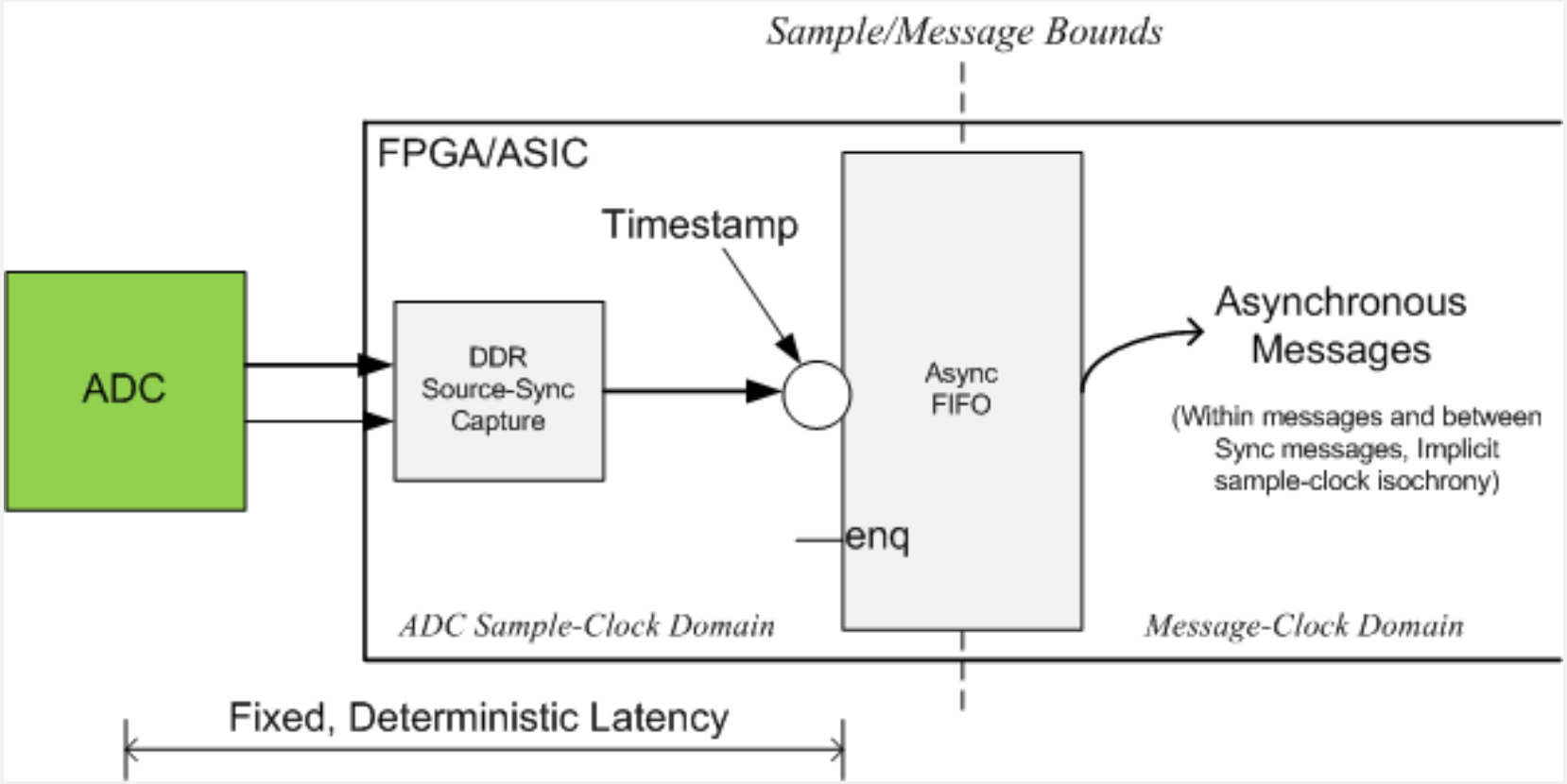
Relativity of Simultaneity

- Speed of light sets a fixed upper bound
- Consider a “logic cell” at the core center of Rubik’s Cube
  - E.g. a simple 6-connected 3D structure
  - 54-connected if you want, still…
- What qualities might a naïve FPGA like this have?
  - What would its clock spine look like?

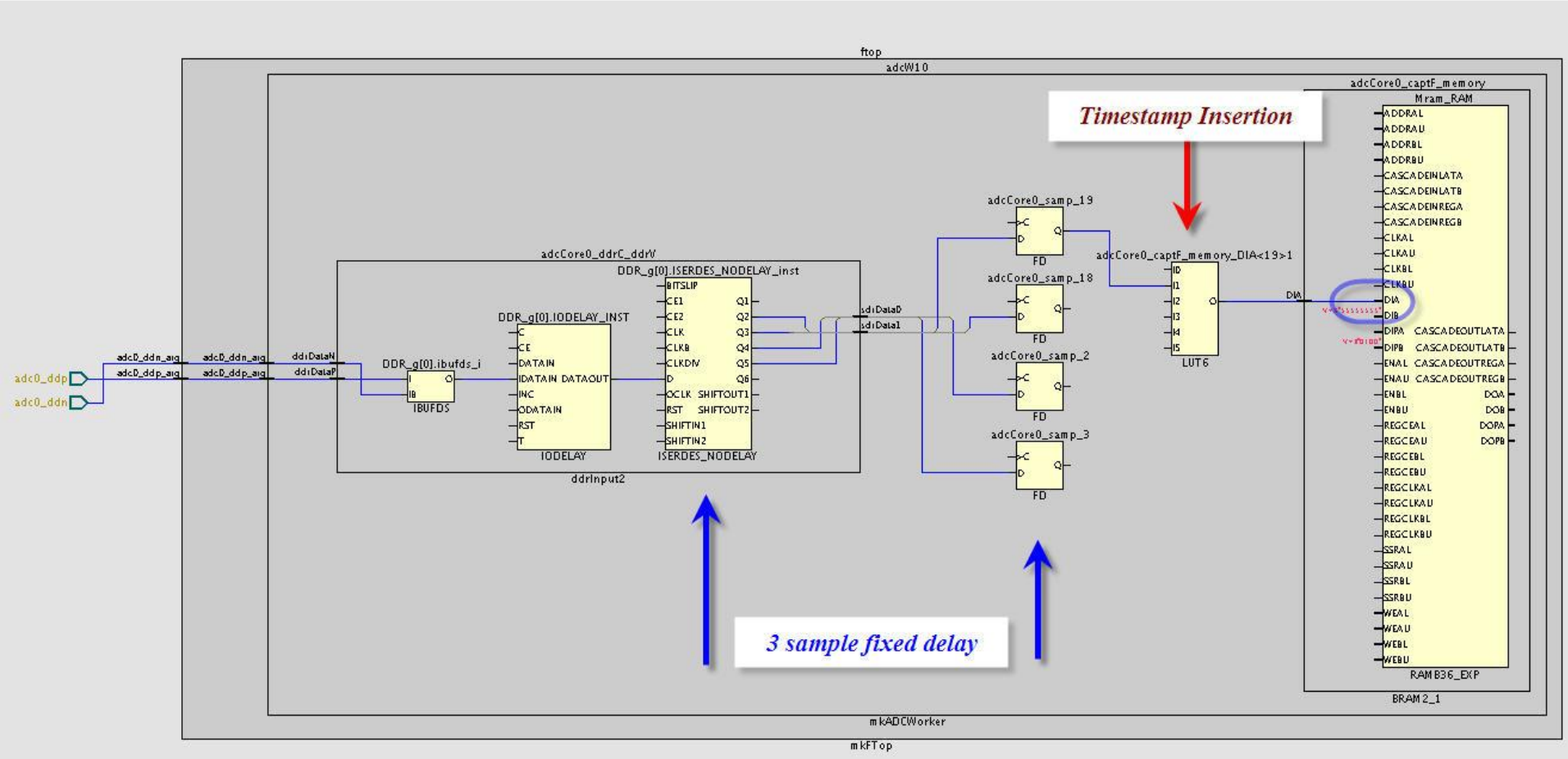
Elastic Pipelines

- Not new, but more important than ever
  - KPNs, SDF, Lee, many others
- Latency Insensitive Design
- A favorite Satnam quote
- Bring more of the Isochronous (real time) world to the Asynchronous
- Brittle is usually bad

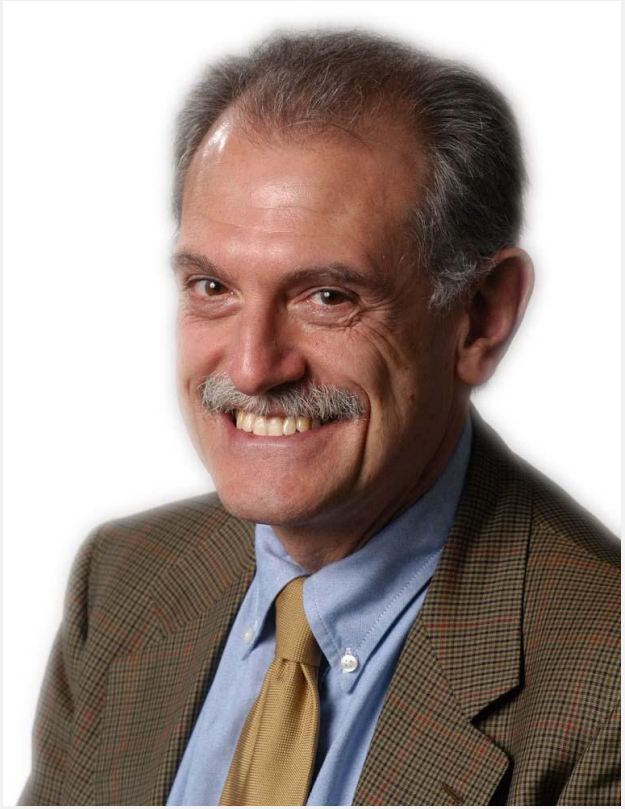
Isochronous and Asynchronous



Winning Lower Latency



Platform Based Design



- ASV was right in 2002
- Stands correct in 2012
- Good bet going forward

Components

- Let components compose
- Keep Divide and Concur in our “bag of tricks”
- Arbitrary Composability
- Linear Effort Property

Circuits as Libraries

- We've heard this before
- Relocation (Spatial Reuse)
- Dynamic Link/Load (Temporal Multiplexing)
- Plenty of runway to make these practical

- What if 10% of a GPP Cache Area were FPGA? (Arvind)

What Might Surprise Us

- Services over Systems
- The “Red Hat” of (FPGA) IP?
- An Open-Source FPGA “App Store”
  - With for-profit support services

What Might Fail Us

- Large bets that don't measure along the way
- Bets on the world not changing
- Bets on global homogeneous scale
- Bets on a single programming paradigm

Summary

- Terribly Optimistic on the trend lines
- End of Si-Moore is someone's problem (ITRS)

- We are bright, thriving community
  - But must continually keep challenging ourselves

- What challenge are you advancing today?
  - When can you share your insights!

Thank You