FPGA 2012

FPGAs in 2032: Challenges and Opportunities in the next 20 Years

Workshop Chairs: Vaughn Betz and
Lesley Shannon

Conference Supporters:

20 Years of the FPGA Symposium

- First Symposium:
  - 1992, Berkeley, CA
  - 148 pages
- FPGA 2012
  - 20th anniversary
  - Monterey, CA
  - ~300 pages

FPGA 1992

- "A High Density, High-Speed, Array-based PLD"
  - Altera EPM7256
  - 256 macrocells (or gates); ~1200 and-gates (pterms)
  - Today: > 1 million logic elements / chip
  - > 1000x density
- "FIR filters with the Xilinx FPGA"
  - 9 cycles @ 12.5 MHz for 8-tap (by 8-bit) FIR
    - 1.4 MHz sample rate, ~11 MMAC/s
  - Today: > 3 TMAC/s
    - > 30,000x throughput

FPGA 1992

- Design style
  - Schematic entry dominant
- Many CAD and architecture papers
  - On logic and routing fabric
  - On logic synthesis, placement, routing, partitioning
- Nothing on system-level
  - Beyond logic & routing
  - CAD above logic synthesis

FPGAs in 2032

- What will they look like?
- What should we research to get there?

The Future: Some Questions

- How do we express designer intent, when we have 100 billion transistors?
- What is the software flow?
- Will CMOS stop at 7 nm? At 3 nm? What then?

More Questions

- Will there be one big programmable chip with processors, hard-logic, programmable interconnect, etc? What is the architecture?
- How do we handle unreliable transistors?
- 3D integration and optical integration – what and how?

All Star Panel

- Mr. Bob Blainey
  - IBM Fellow, Compiler and Next-Generation System Software
- Dr. Ivo Bolsens
  - CTO and Senior Vice-President, Xilinx
- Dr. Misha Burich
  - CTO and Senior Vice-President, Altera
- Professor Peter Cheung
  - Head, Dept. of Electrical and Electronic Engineering, Imperial College
- Dr. Michael Flynn
  - Chairman, Maxeler Technologies and Professor Emeritus, Stanford
- Mr. Shep Siegel
  - Founder and CTO, Atomic Rules
- Dr. Steve Teig
  - President and CTO, Tabula

Misha Burich

- Senior Vice President & CTO, Altera Corporation
- Managed all R & D for Altera's FPGA architectures, HardCopy ASICs, software, embedded processors and IP
- Served as VP of R & D at Cadence, Mentor Graphics and Silicon Compiler Systems
- Co-founder of Silicon Design Labs in 1984
- Started career at Bell Labs in 1978
- M.S. and PhD in EE from U. of Minnesota and Dipl. Eng. from the University of Belgrade

Bob Blainey

- IBM Fellow
- Technical architect for workload-optimized systems in IBM Software Group
- > 20 years at IBM
  - Focus on deep optimization of software for IBM systems
- Extensive work on program transformations for parallelism and high performance
- Recent focus on re-imagining the relationship between software and hardware in the post-scaling world
  - Both short-term optimizations and new system structures using disruptive technologies

Steve Teig

- President and CTO, Tabula
- Inventor of Tabula's Spacetime 3-D Programmable Logic Arch.
- Previously CTO of Cadence
- CTO of Simplex Solutions, where he invented the X Architecture
- Co-founder of two successful biotechnology companies: CombiChem (CTO), and BioCAD (CTO and later CEO)
- 1980's: key logic simulation and place-and-route technologies
- B.S.E. degree in EE & CS from Princeton University
- Holds over 240 patents.
- 2011: World Technology Award for IT hardware innovation

Michael Flynn

- Professor Emeritus at Stanford
- Chairman of Maxeler Technologies
  - US and UK based company dedicated to maximum performance computing
- Directed the Architecture and Arithmetic group at Stanford for more than 20 years
- Flynn taxonomy
- Eckert-Mauchley and Harry Goode Memorial Awards in 1992 and 1995, respectively
- Fellow of the IEEE and the ACM

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Thank you for coming

Panel Presentations: Part II

- Dr. Ivo Bolsens
  - CTO and Senior Vice-President of Xilinx
- Mr. Shep Siegel
  - Founder and CTO of Atomic Rules
- Professor Peter Cheung
  - Head of Department of Electrical and Electronic Engineering, Imperial College London

Dr. Ivo Bolsens

- Senior VP and CTO, Xilinx
- Responsible for advanced technology development, Xilinx research labs and Xilinx university program
- Previously VP of information and communication systems at IMEC
  - Research interests in VLSI verification, DSP applications and hardware, wireless communications, HW/SW co-design and SoC design
- PhD in Applied Science and MSEE from the Catholic University of Leuven, Belgium

Mr. Shep Siegel

- Founder and CTO of Atomic Rules, 2008
- 30 years of practice in system architecture, applied DSP and circuit design
- 7 years at Mercury Computer, leading FPGA technology group
  - Drove company-wide adoption of IP standards like OCP and Bluespec System Verilog
- Principle Design Engineer at Datacube
  - Invented Adaptive Zonal Coder, cited by over 100 image and video processing patents
- BSEE from Rochester Institute of Technology
- In the 80's, he won an "outstanding engineering" Emmy

Professor Peter Cheung

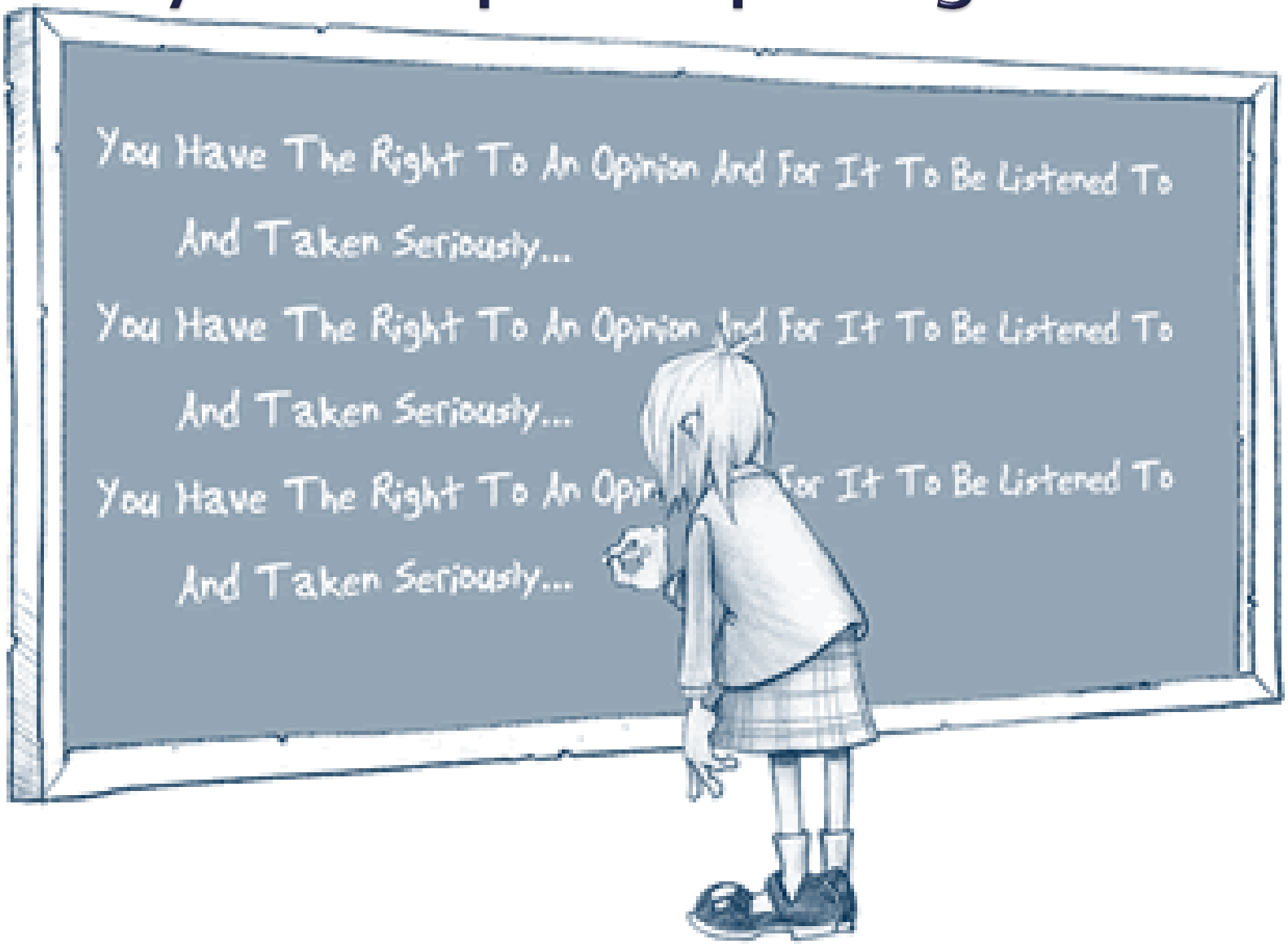
- Professor and Chair, Dept. of Electrical Engineering, Imperial College London
- Recent research into variability, reliability and degradation issues relating to FPGAs
- First went to Imperial College as a undergrad student in 1970
  - Apart from 3 short years working for Hewlett Packard, stayed there ever since
- When Wayne Luk moved from Oxford to Imperial in 1995, he and Peter joined forces together to build the FPGA team at Imperial.
  - Has 6 Faculty members and ~25 Research Assistants and PhD students.

20 minute Breakout Session

- We ask you to divide into sub-groups to discuss the presentations
- Please prepare a question for the presenters

Questions for the Panel

Thank you for participating



Wrap up

- Thank you all for your participation
- Registration for the conference opens at 6pm
- The Reception starts at 7pm
- The conference starts at 8:40am tomorrow
  - Breakfast/Registration at 8am

Thank You to Our Supporters

See you at FPGA 2013's Workshop!