Fully-Functional FPGA Prototype with Fine-Grain Programmable Body Biasing

Masakazu Hioki[1], Toshihiro Sekigawa[1], Takashi Kawanami[2],
Yohei Matsumoto[3], Tadashi Nakagawa[1],
Toshiyuki Tsutsumi[4] and **Hanpei Koike**[1]

[1]National Institute of AIST,
[2]Kanazawa Institute of Technology
[3]Tokyo University of Marine Science and Technology
[4]Meiji University

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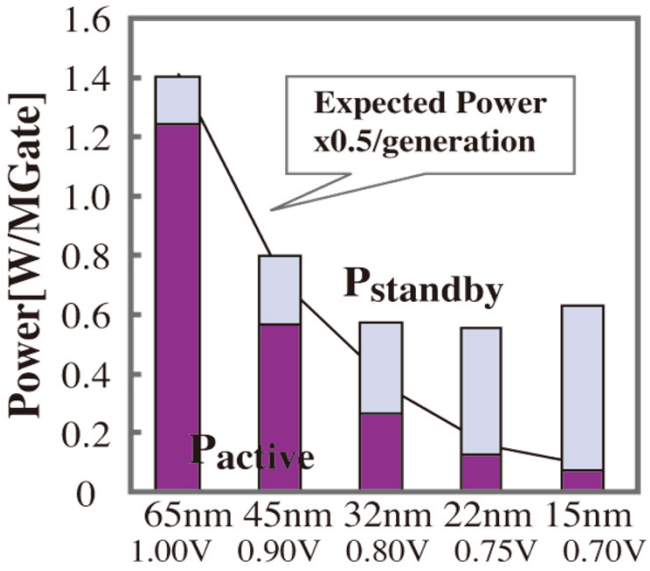
Outline

- Introduction
  - Static leakage power problems
  - Flex Power FPGA = FPGA with fine-grained programmable body biasing
- Flex Power FPGA Test Chip Design
  - Architecture
  - Fine-grain programmable body biasing circuits
  - CAD Flow
- Test Chip Evaluation Results in Silicon
  - Static Power Measurement
  - Implemented Ring Oscillator Frequency/Power Measurement
  - Area Breakdown
- Conclusions

Static Leakage Power Problem

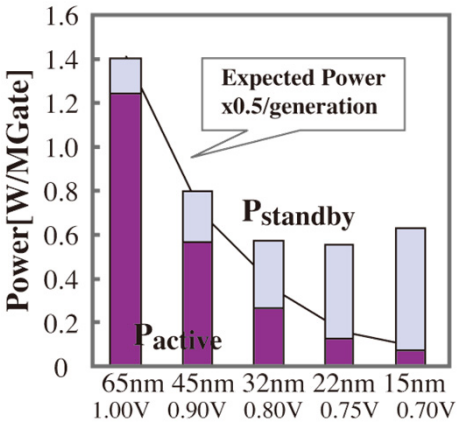
- As the technology node becomes smaller, static leakage power has emerged as the more serious problem than traditional dynamic ($1/2CV^2$) power consumption.
- New Trends: Sub-threshold / Near-threshold Operation



From Morifuji et.al., IEEE Trans. on E.D., Vol.53, No.6, June 2006

More Serious in FPGA

According to the Device Scaling, Static Leakage has become Serious Problem



Morifuji et.al., IEEE Trans. on E.D., Vol.53, No.6, June 2006

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Static Leakage in FPGA is More Serious

FPGA vs. ASIC	
Area	40:1
Critical Path Delay	3.2:1
Dynamic Power	12:1
Static Power	87:1

Kuon and Rose, *Measuring the Gap Between FPGAs and ASICs*, FPGA 2006, Feb. 2006

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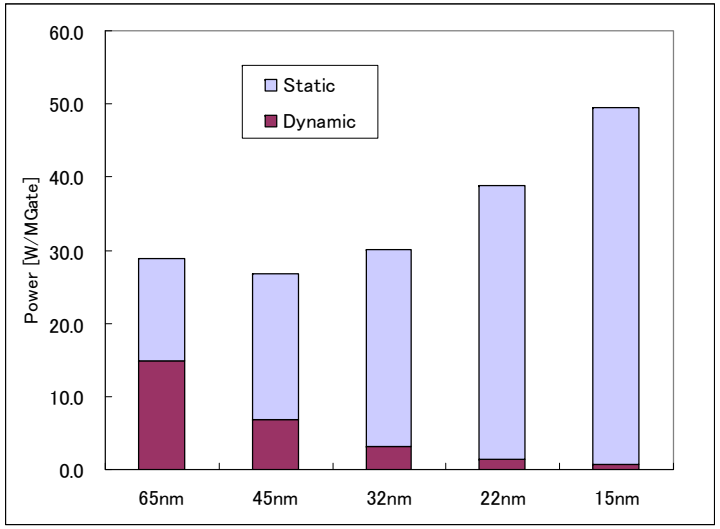
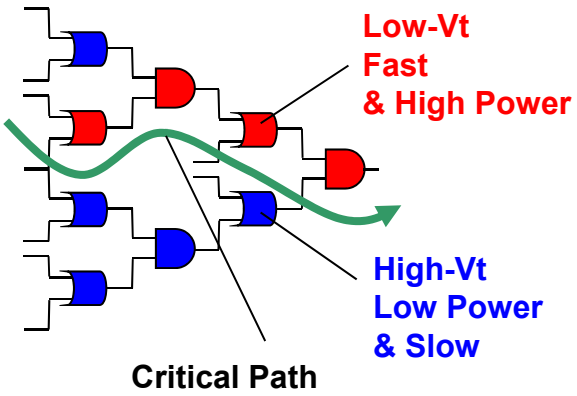
Prediction of FPGA Power Consumption
（Dynamic Power 12x、Static Power 87x）

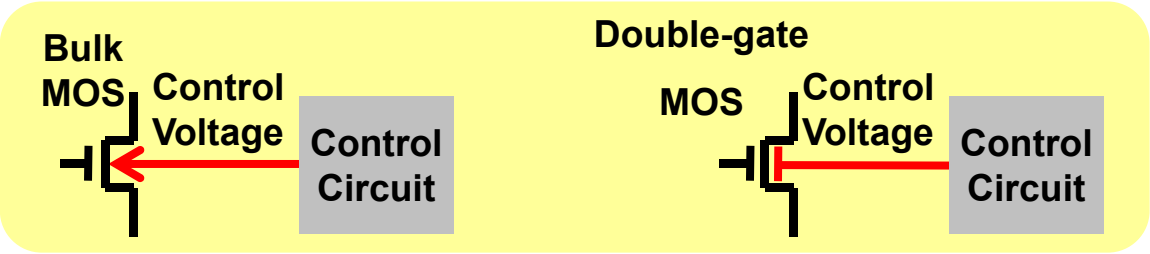


Standard Solution: Vt Optimization

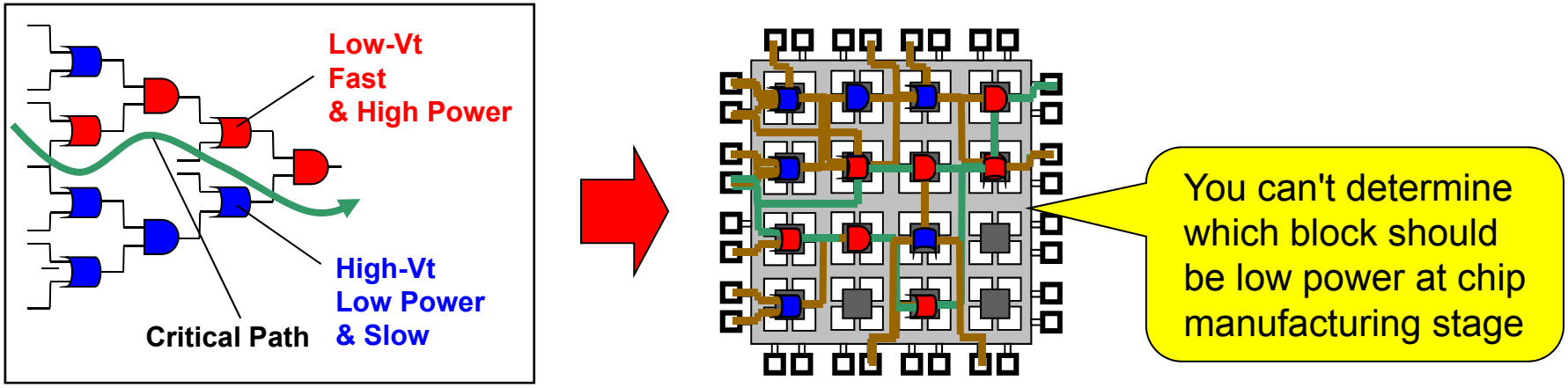
- Threshold voltage (Vt) optimization techniques is the standard solution to reduce leakage power
  - Using Low-Vt on critical path circuit *only*



- How can we control the Vt of a transistor?
  1. Process Tuning (Setting the Vt at Fabrication)
     - Dual Vt, Triple Vt ...
  2. Body Biasing (Controlling the Vt Electrically)
     - Applying well bias voltage to the body part



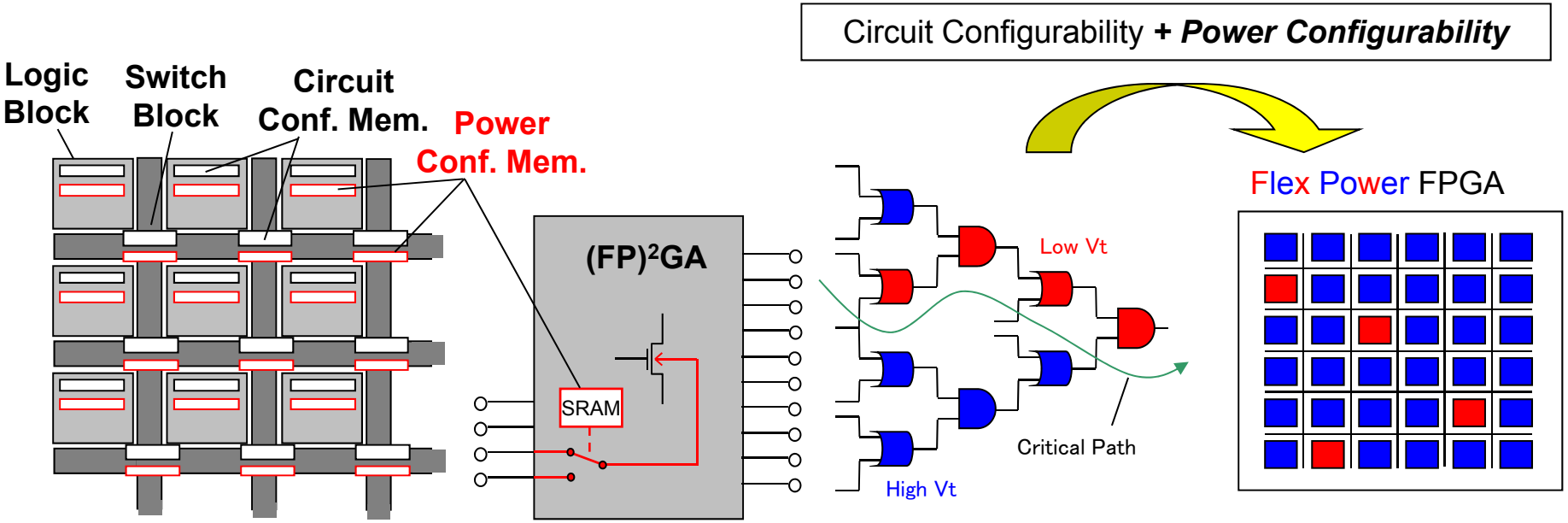
Vt Optimization Technique on FPGA?



Vt should also be programmable

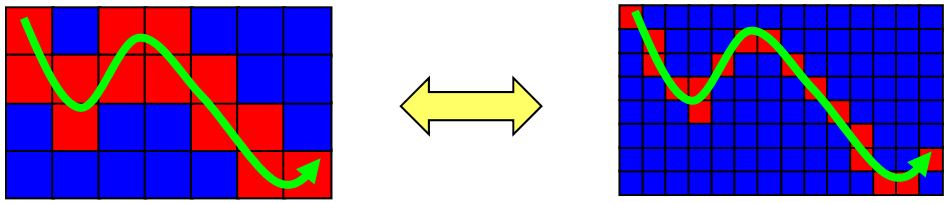
(FP)^{2}GA : Flex Power FPGA

- Flex Power FPGA uses Body Biasing technique to design a power configurable logic block and switch block with power configuration SRAMs to control the speed and static power consumption trade-off.
- Flex Power FPGA provides power configurability as well as circuit configurability.



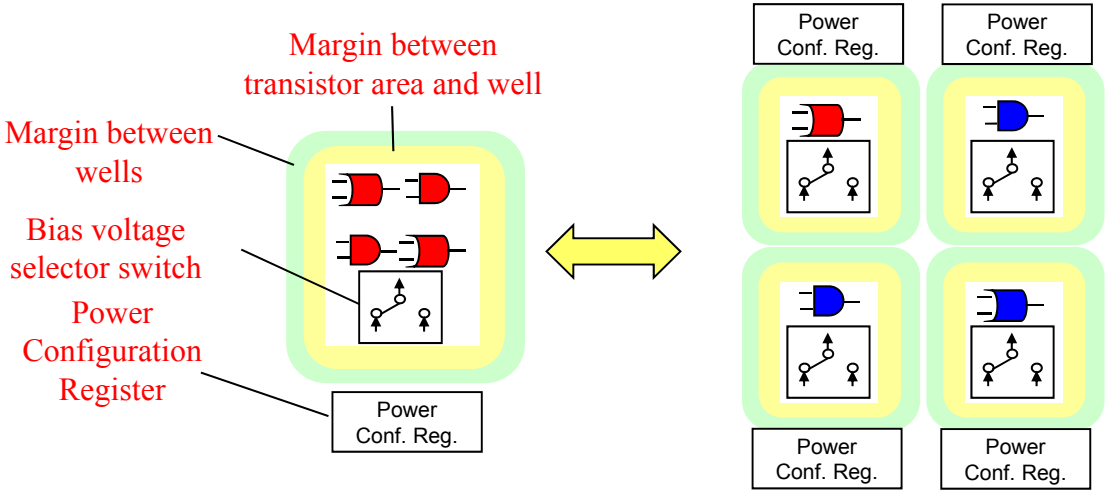
Vt Control Granularity

- The Finer, The Cooler
  - exact carving of Small Hot Circuit from Huge Cool Circuit

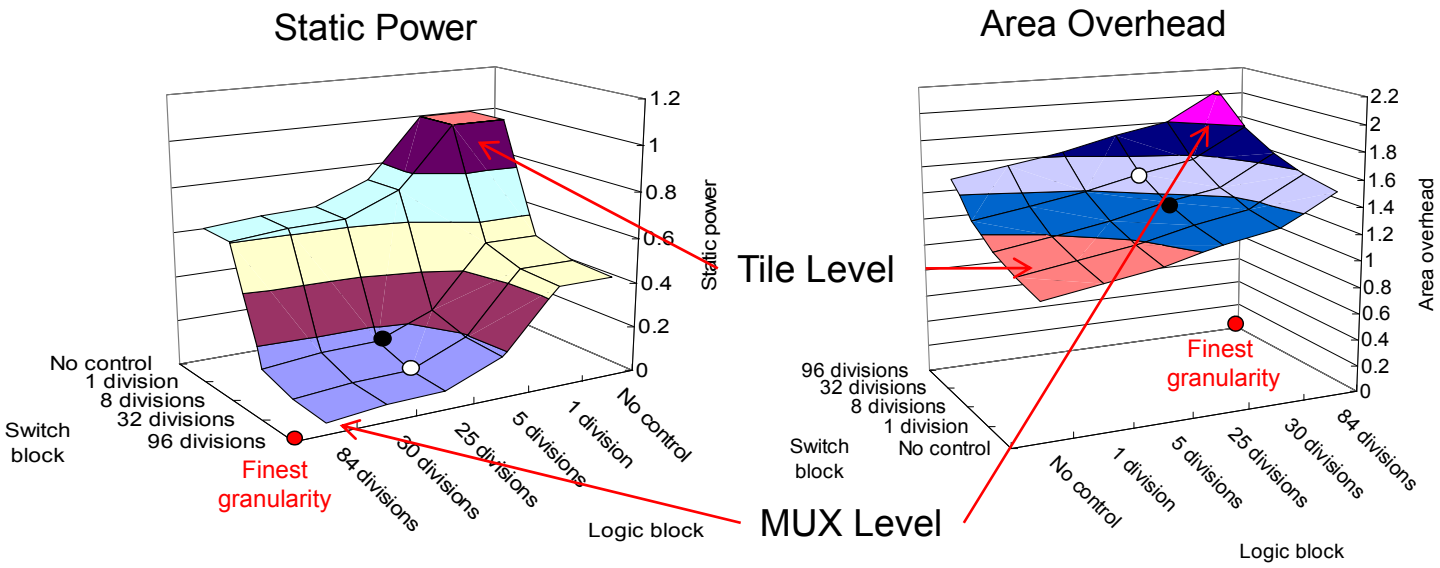


e.g. Tile Level e.g. MUX Level

- Problem: Area Overhead
  - Additional Vt control circuits area & Well separation area



Early Evaluation on Static Power Reduction and Area Overhead v.s. Vt Control Granularity (Hioki, et.al., FPT06)



- Evaluation based on simple signal, power and area models
- Combinations of different Vt divisions in logic block and switch block

Early MCNC Benchmark Simulation Results (Kawanami et.al. IEICE 2004/FPGA2004 poster)

Low−Vt Ratio ≈ 1.3%

Ioff in Hi−Vt ≈ 1/50

$1 \times 1.3\% + 1/50 \times 98.7\% \approx 1/30$

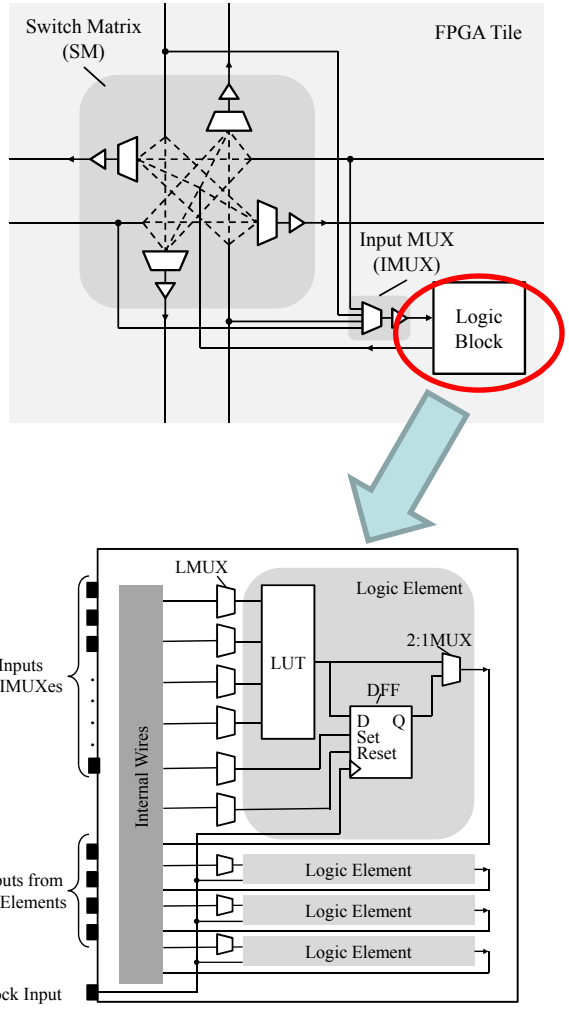
Vt controllability performance of the transistor
Bias voltage range

Nature of the application circuit
Vt control granularity (Architecture)

- Can it be true with real chip?
- How much area overhead for fine-grained body biasing? Can we improve it?

Flex Power FPGA Test Chip Architecture

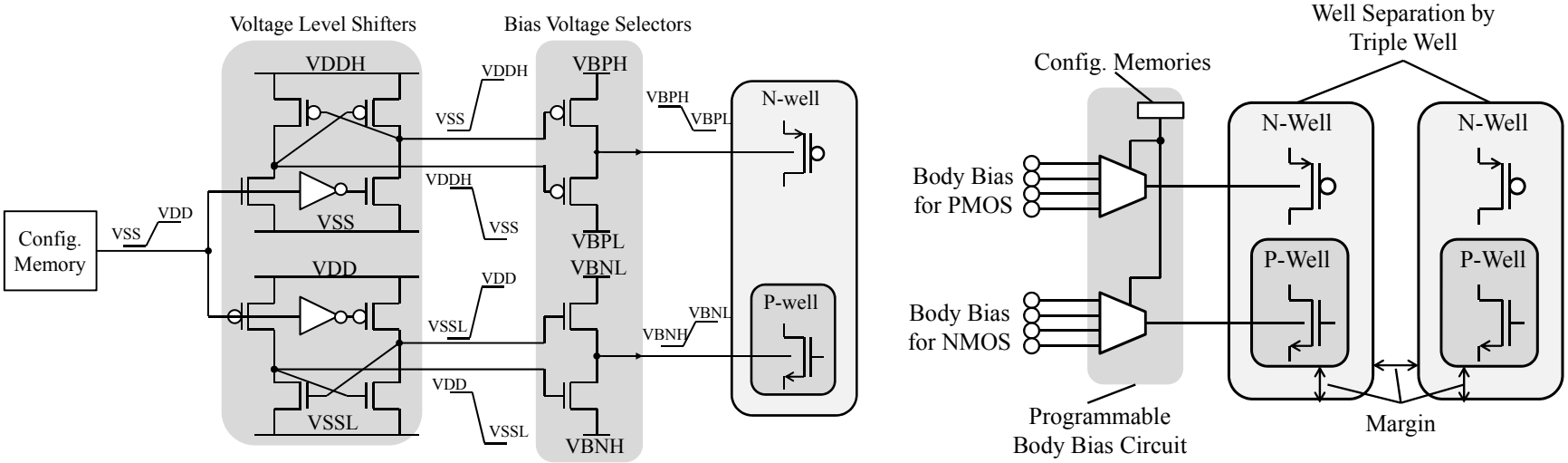
- Simple island-style and tileable FPGA
- Programmable interconnects with unidirectional and single-driver routing architecture
- A switch matrix with disjoint topology
- Logic block containing 12 IMUXes, 24 LMUXes and 4 logic elements
- A 4-input LUT, a D-FF with set and reset and a 2:1MUX per Logic Element
- Combined IO function to reduce design effort



MUX-level Fine-Grain Programmable Body Biasing

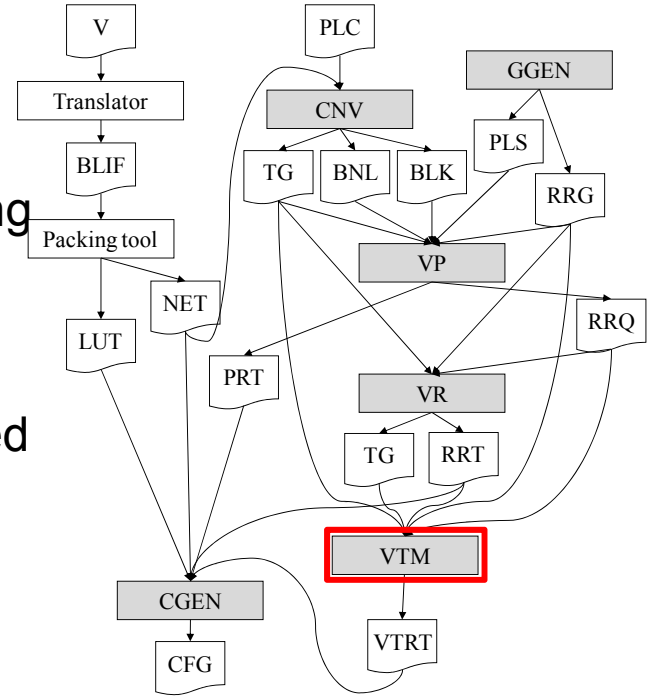
- Body bias voltage in 57 elemental circuits in a FPGA tile (8 SMUXes, 12 IMUXes, 24 LMUXes, 4LUTs, 4 DFFs, 4 2-1MUXes and a PAD Output MUX) can be individually controlled by dedicated programmable body biasing circuits

- Overheads for fine-grained body bias programmability:
  - Additional programmable body bias circuit for each elemental circuit
  - Triple well separation to apply body bias voltage to each MOSFET's body individually.



Flex Power FPGA CAD Flow

- Original Flex Power FPGA CAD tools are newly developed.
- VTM automatically maps Vt according to the slack analysis
- Successfully Formal-Verified using modest-size application such as microprocessor core
- Interfaces to the standard commercial CAD tools are included
- Why not VPR (4.3)?
  - Unidirectional Wire
  - 3D Extensibility
  - e.t.c.

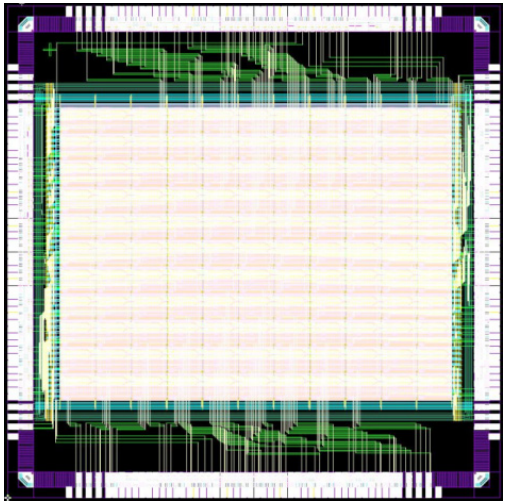


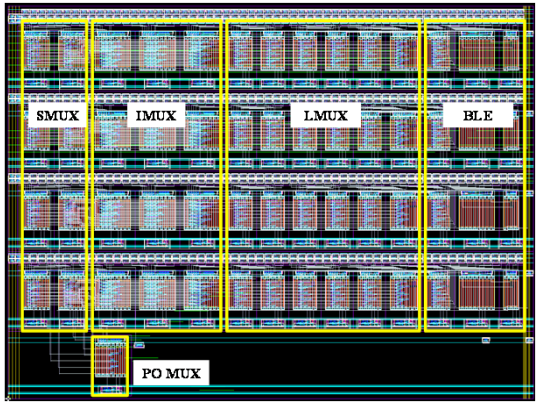
Software	
GGEN	RRG and PLS generator
CNV	NETto BNL transformer TG and BLK generator
VP	Placer
VR	Router
VTM	Vth mapper
CGEN	Config. bit stream generator

File	
V	Verilog RTL netlist
BLIF	Gate level netlist
NET	CLB netlist
LUT	LUT truth table
PLC	Pad location
TG	Timing graph
BNL	VP inputtable netlist
BLK	Fix block location
PLS	Function block location
RRG	Routing resource graph
RRQ	Routing resource request
PRT	Placement result
RRT	Routing result
VTRT	Vt map result
CFG	Config. bit stream

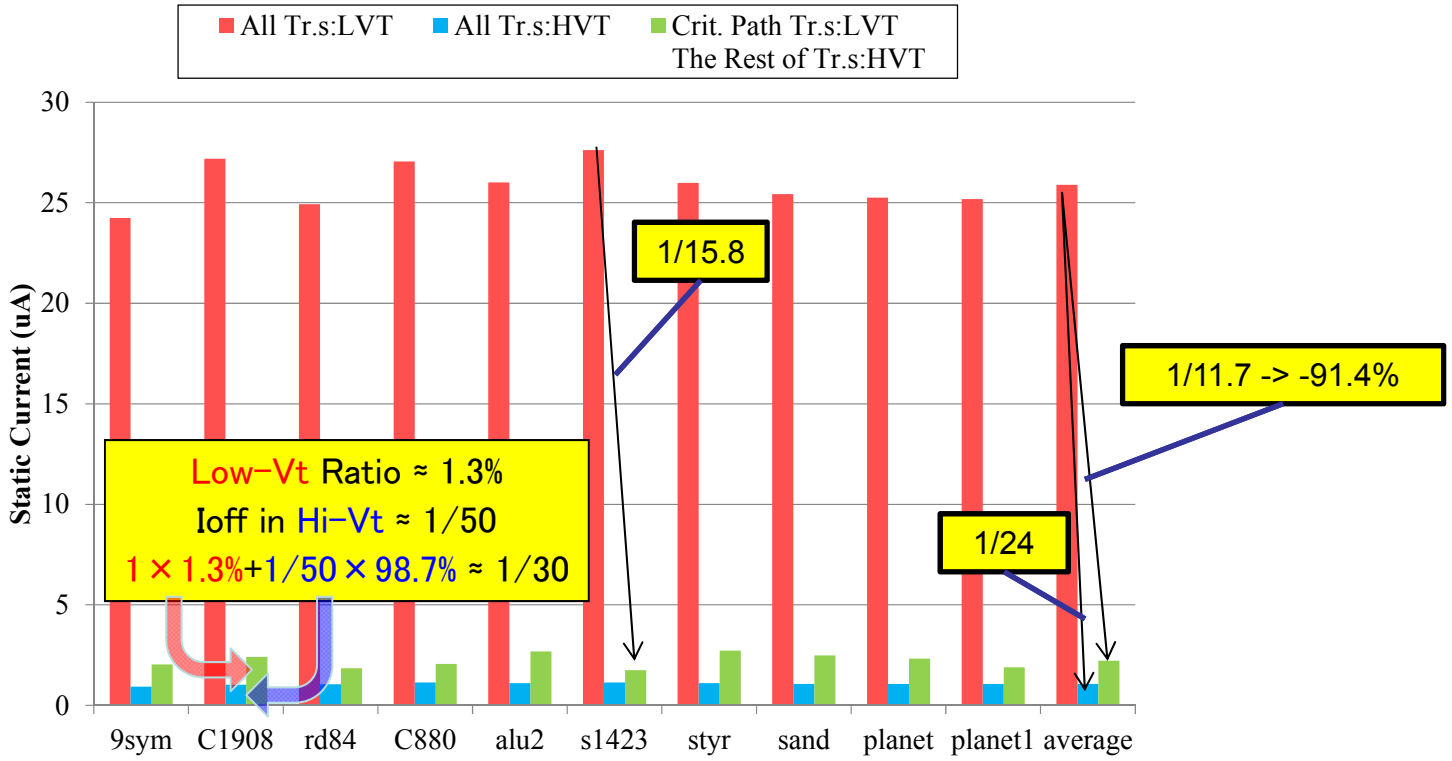
Flex Power FPGA Test Chip Fabrication

- Fabrication process :1P9M 90-nm low-power bulk CMOS process technology.
- 11 × 11 FPGA tile array size : 3.2 mm × 2.4 mm
- The FPGA tile size : 290 um × 217 um
- The main elemental circuits of FPGA such as buffers and MUXes use built-in low threshold voltage (LVT) MOSFETs.
- Configuration memories and configuration shift registers use built-in high threshold voltage (HVT) MOSFETs.
- Transistor count : 1.34 million transistors, including chip I/Os.
- The total number of body biasing domains is 6,897 (57x11x11)
- Totally Manually Laid-out.



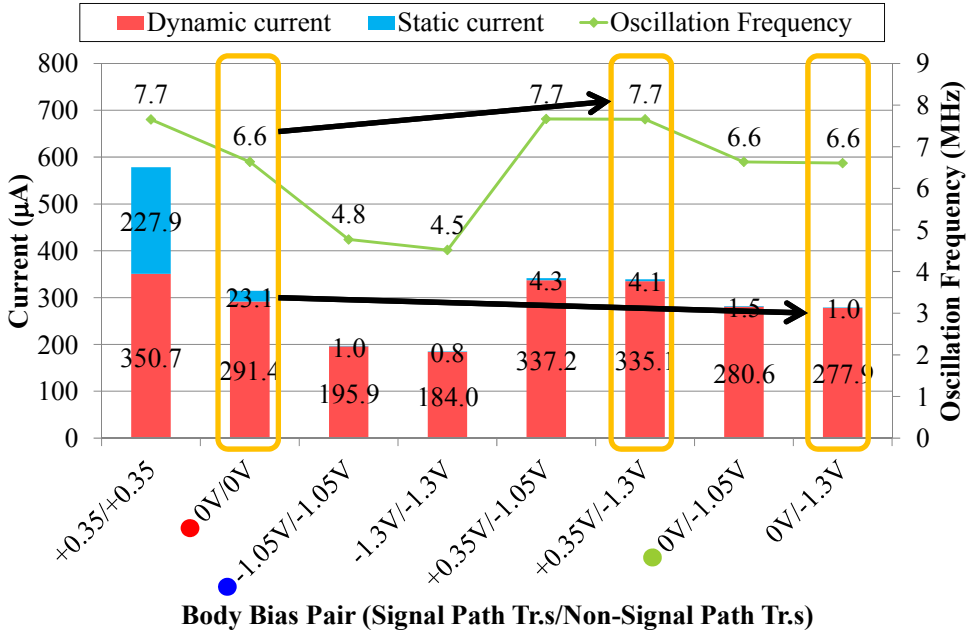


Measured Static Current with 10 ISCAS Benchmark Circuits



- 10 biggest ISCAS Benchmark circuits fittable to the size of the FPGA test chip
- 3 different Body Biasing Configurations: ALL LVT(0V), ALL HVT(-1.05V) and FLEXPOWER
- Static current decreases down to 1/24 from ALL LVT to ALL HVT
- With FLEXPOWER , static current decreases by 1/15.8 at the maximum (s1423 circuit) and 1/11.7 in average

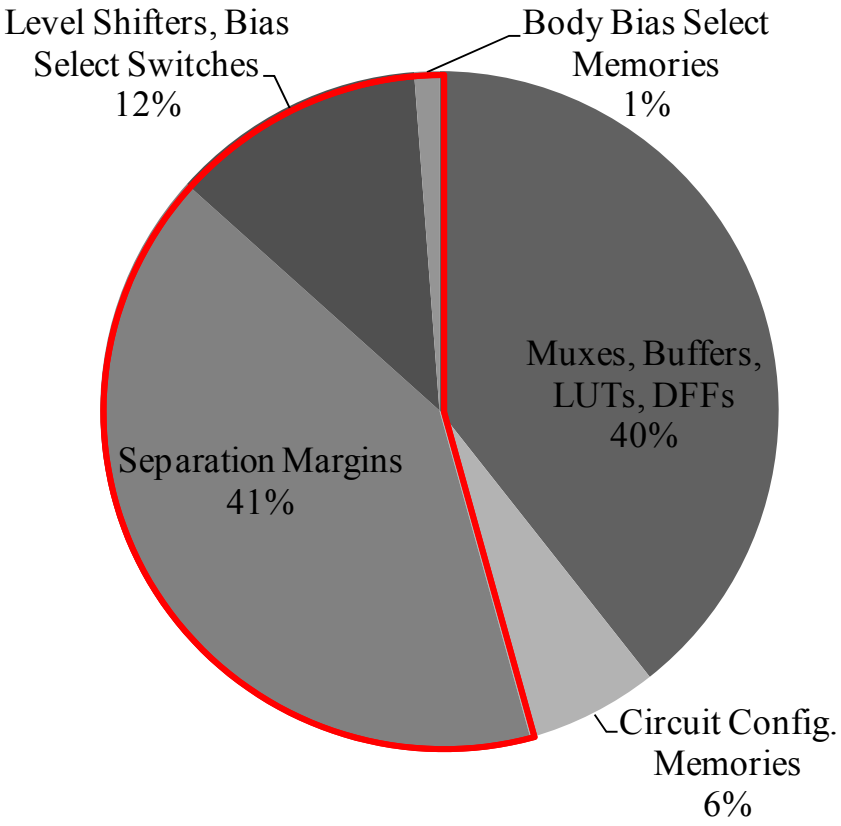
Measured Result of Implemented 22-Stage Ring Oscillator



- Dynamic / Static Currents and Oscillation Frequency of a Ring oscillator
- Body Biasing Conditions: Combinations of Zero (0V) or Forward (0.35V) Biasing for LVT, and Reverse (-1.05V) ore Deeper (-1.3V) Reverse Biasing for HVT
- The static current decreases from 23.1 uA to 1.0 uA without affecting 6.6MHz oscillation
- The oscillation frequency increases from 6.6 MHz to 7.7 MHz by applying Forward biasing.
- By combining Forward biasing with Deeper Reverse Biasing, the increase of total current can be only 8%.(Static current is reduced by 1/5)

Tile Area Breakdown

- Elemental circuits such as MUXes, LUTs, DFFs, buffers, and configuration memories occupy 46% of the tile area.
- The remaining 54 % of the FPGA tile area is occupied by additional elements for fine-grain programmable body biasing.
- In particular, the well-separation margins occupy 41 % of the tile area.
- The finest partition of the body biasing domain of 57 in the FPGA tile doubles the area.
- Further progress in device and process technologies such as deep trench isolation or SOI devices has possibility to reduce the well-separation space dramatically.



Conclusions

- A fully-functional Flex Power FPGA test chip with fine-grain programmable body biasing is successfully fabricated using low-power 90-nm bulk CMOS technology.
- Fabricated FPGA test chip shows drastic reduction of the static current by 91.4% on average, although the FPGA tile area is increased by well-separation margins and programmable body bias circuits.
- Evaluation with implemented ring oscillator shows that the static current decreases from 23.1 uA to 1.0 uA, while maintaining the same oscillation frequency of 6.6MHz.
- The oscillation frequency increases from 6.6 MHz to 7.7 MHz by applying body bias voltage pair of (+0.35 V/–1.3 V) compared to the FPGA with non-body bias condition (0 V/0 V). The increase of total current is only 8%.
- Evaluation results show that the fabricated Flex Power FPGA test chip achieves drastic static current reduction without operation speed degradation.
- Evaluation results also show that the fabricated Flex Power FPGA test chip accelerates the operating speed of implemented ring oscillator without substantial power increase by combining forward body biasing and reverse body biasing techniques.
- Future Work: FD-SOI(SOTB) implementation, area optimization e.t.c.