GROK-LAB: Generating Real On-chip Knowledge for Intra-cluster Delays Using Timing Extraction

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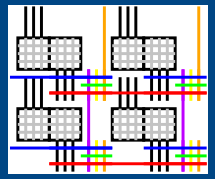
Motivation



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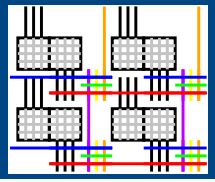

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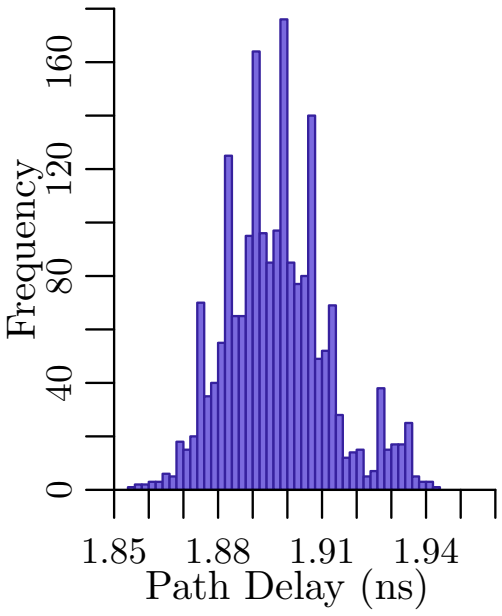
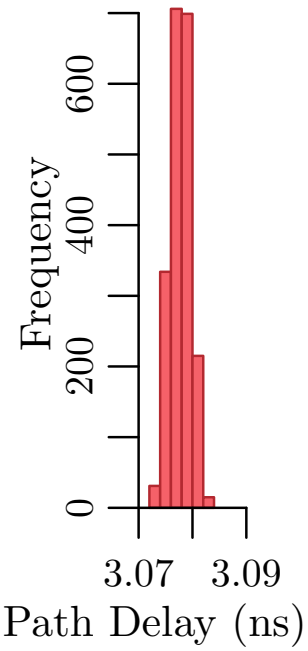


Measured



CAD Tools

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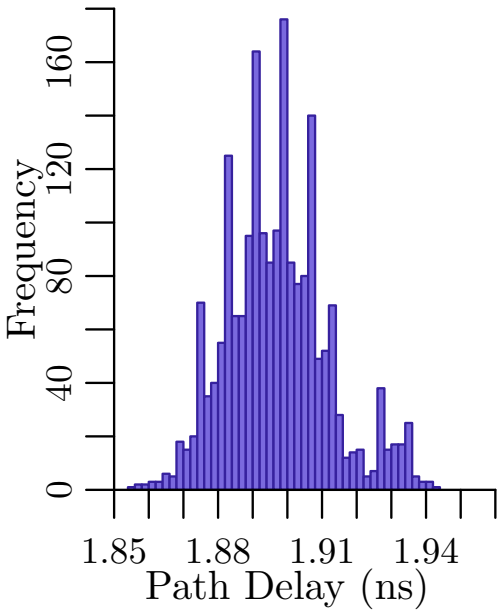
- No correlation between CAD and measurements



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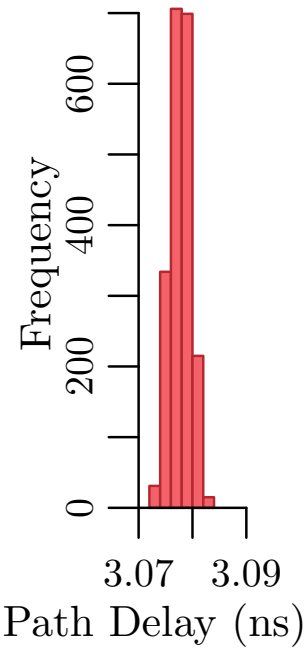

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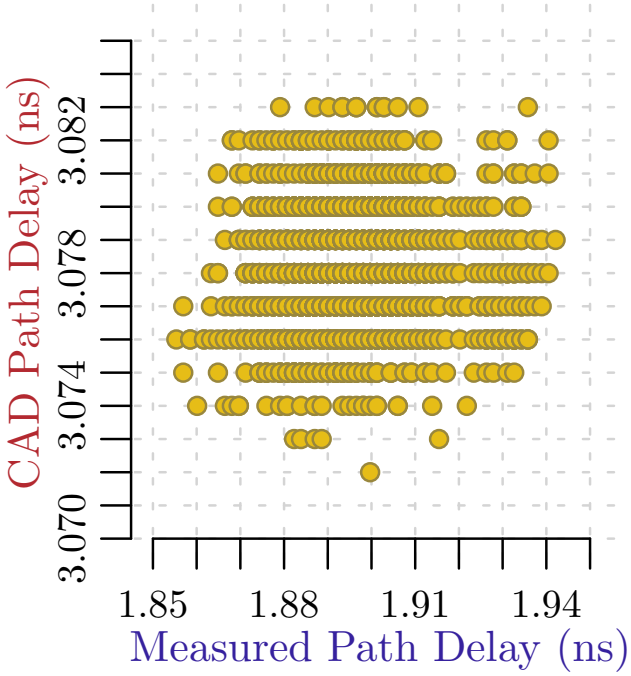

Correlation

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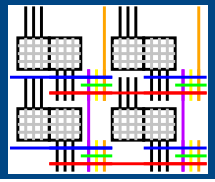

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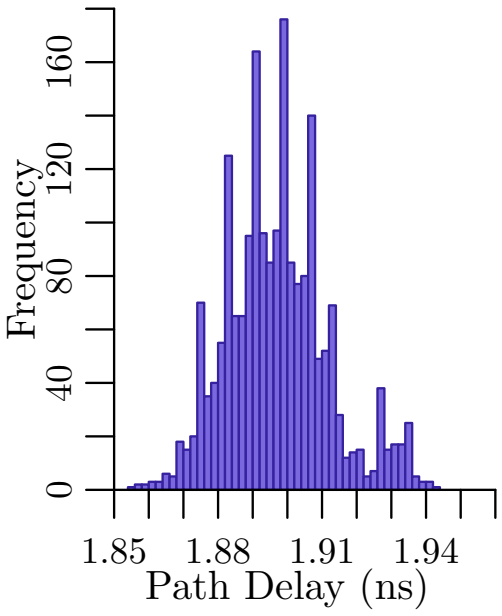

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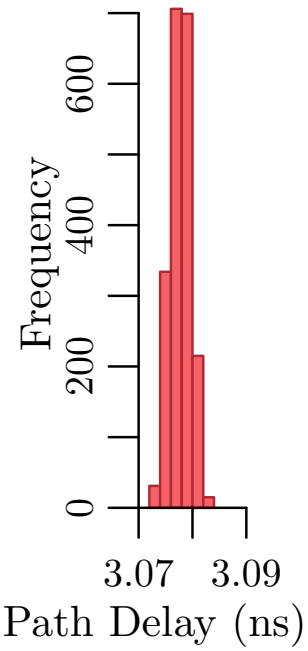

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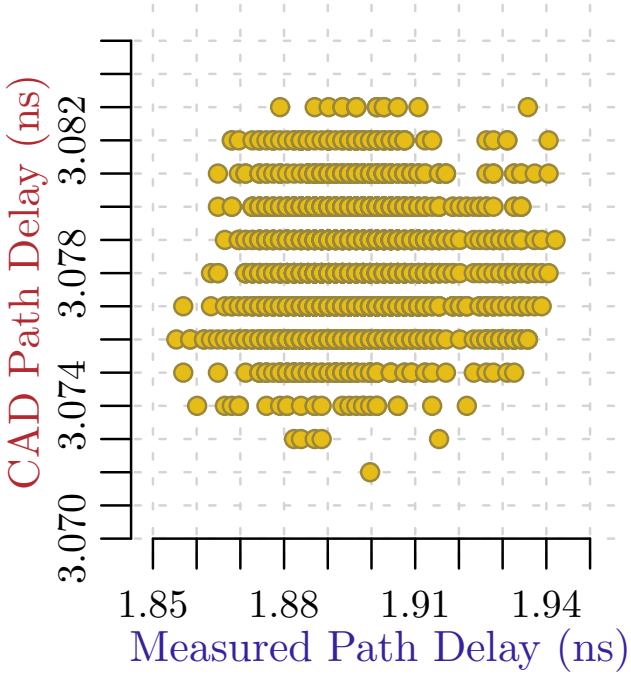

Correlation

- CAD tools unaware of actual distribution
- DVS, etc. cannot take advantage of large distribution

Motivation

Benefit of knowing variation in FPGA

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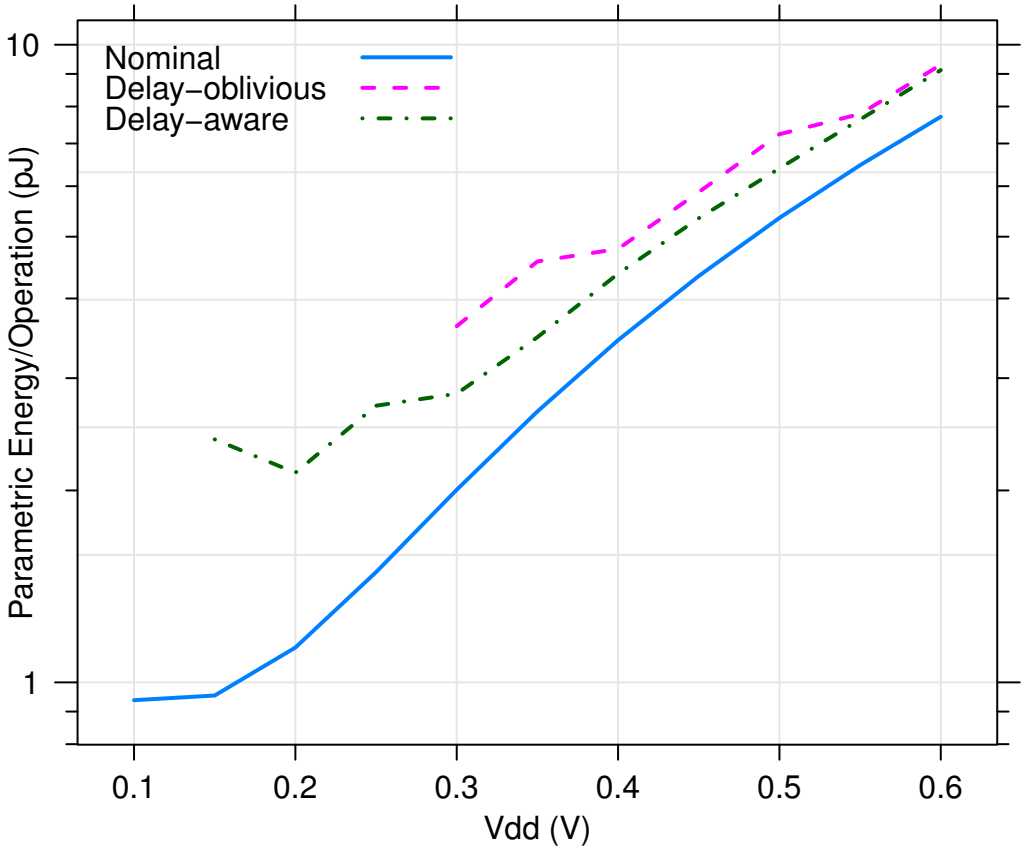
Benefit of knowing variation in FPGA
$\rightarrow$ Perform component specific mapping

Mehta's FPGA'12 limit study

- Eliminate delay margins induced by variation
- Lower energy per operation (1.42-1.98$\times$)
- Benefits increase with technology scaling



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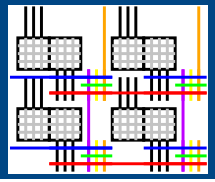


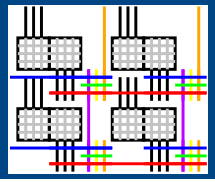
Component specific mapping

- Leverages variation
- Requires fine-grain delay information

Timing Extraction

- Extracts fine-grain delays (LUT-level magnitude)
- Uses only resources available in the FPGA
- Provides detailed process variation characterization

Outline



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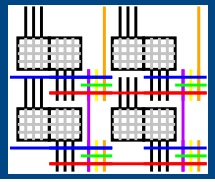

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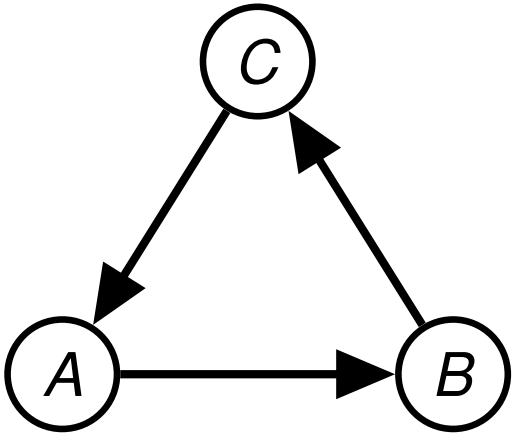

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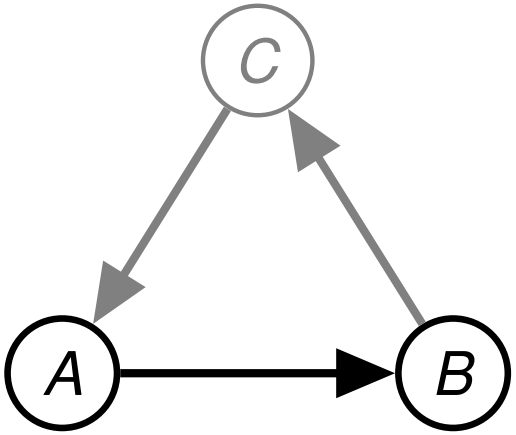

$$A + B = 5$$

Timing Extraction

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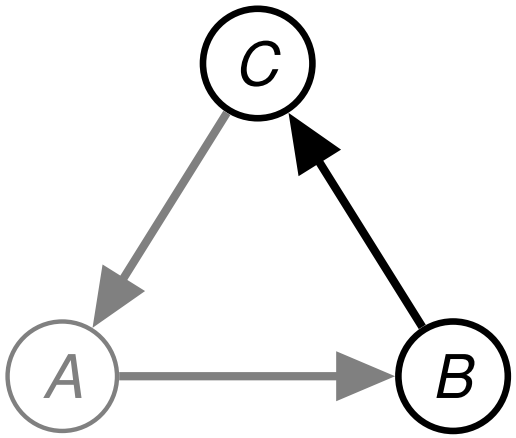

$$A + B = 5$$
$$B + C = 4$$

Timing Extraction

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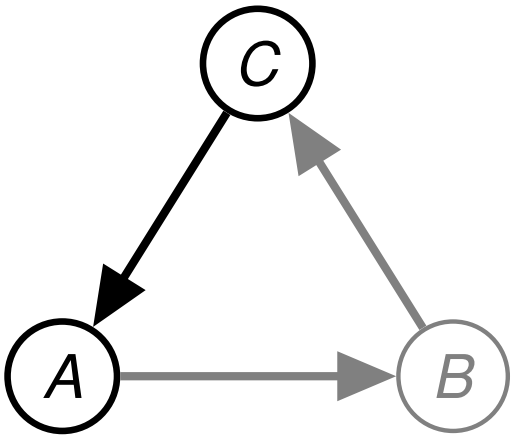
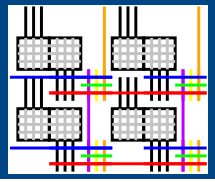


$$A + B = 5$$
$$B + C = 4$$
$$C + A = 3$$

Timing Extraction



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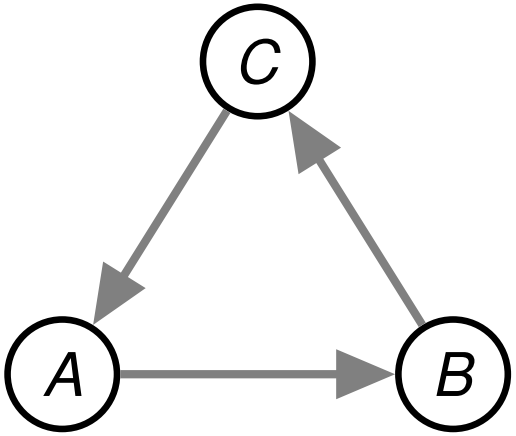

$$\begin{aligned} A + B &= 5 \\ B + C &= 4 \\ C + A &= 3 \end{aligned} \quad \Rightarrow \quad \begin{aligned} A &= 2 \\ B &= 3 \\ C &= 1 \end{aligned}$$

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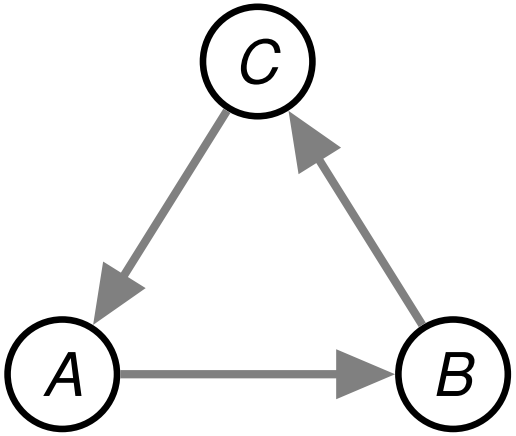

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- Must carefully define what forms a component

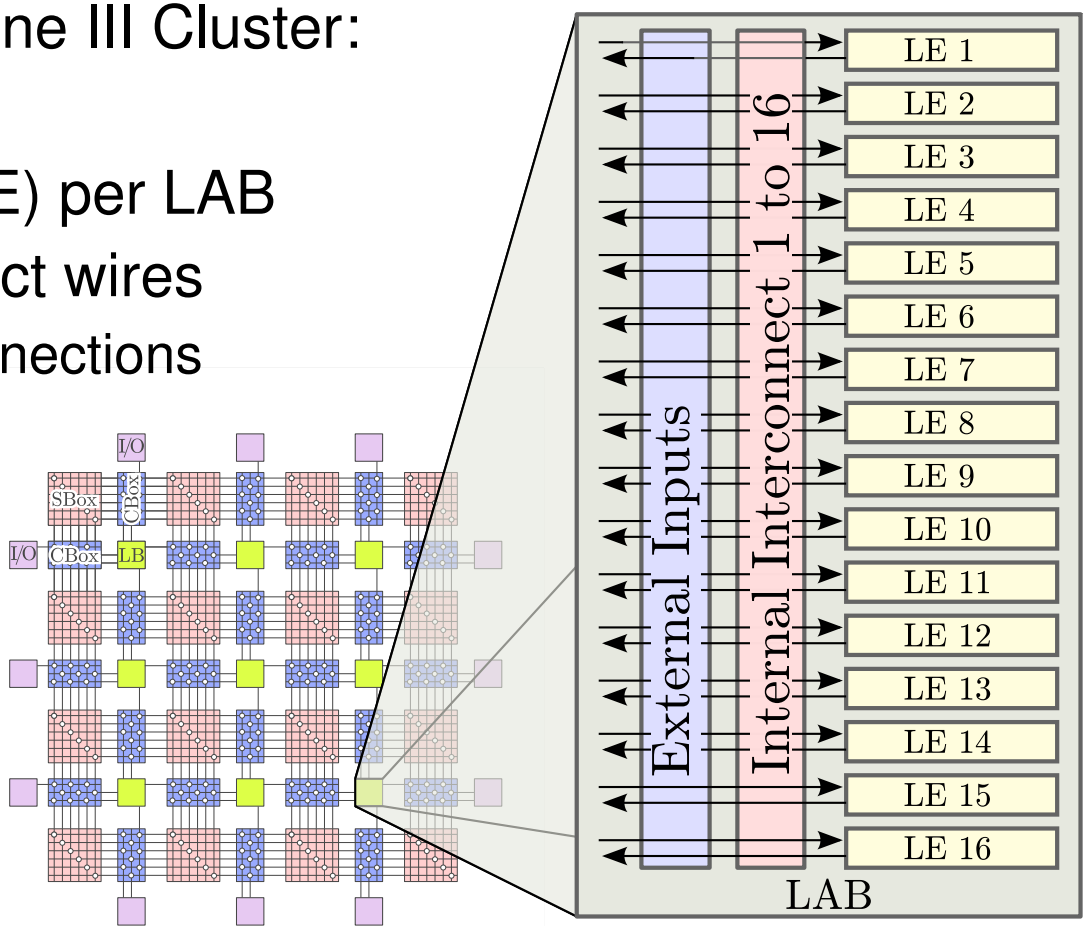
Grounding

Timing Extraction generally applicable to FPGAs

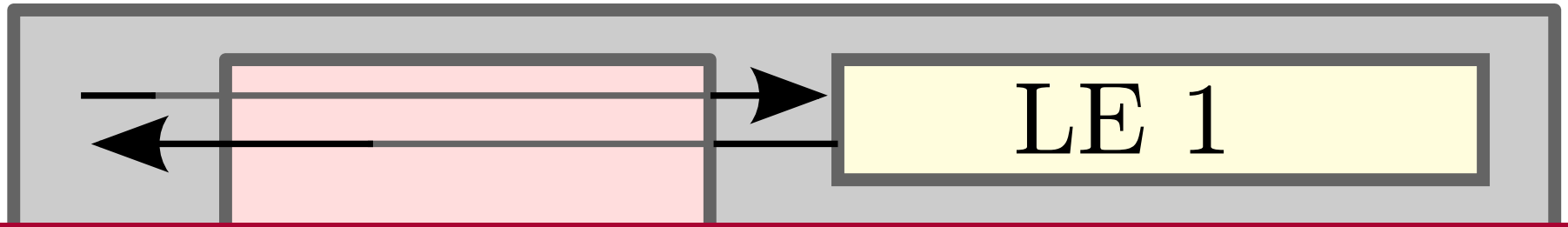
- Registers
- Configurable clocks

Grounding on Altera Cyclone III Cluster:
Logic Array Block (LAB)

- 16 Logic Elements (LE) per LAB
- 16 Internal interconnect wires
  - Local LE to LE connections
- External input wires
  - Not measured



Cyclone III LAB Architecture



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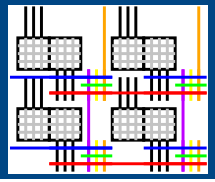
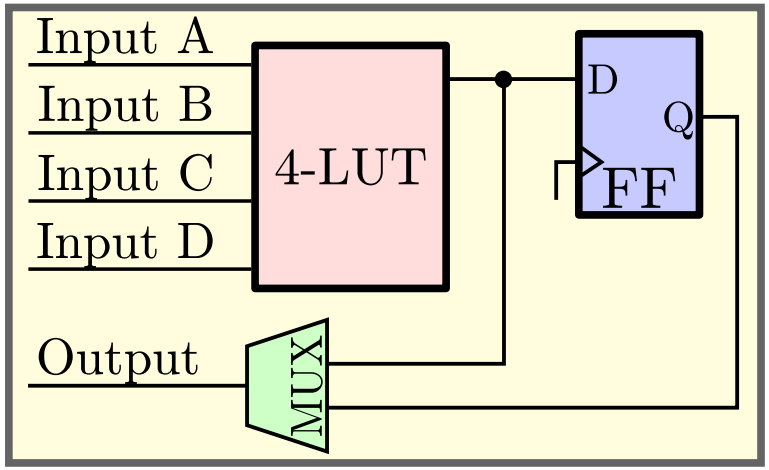
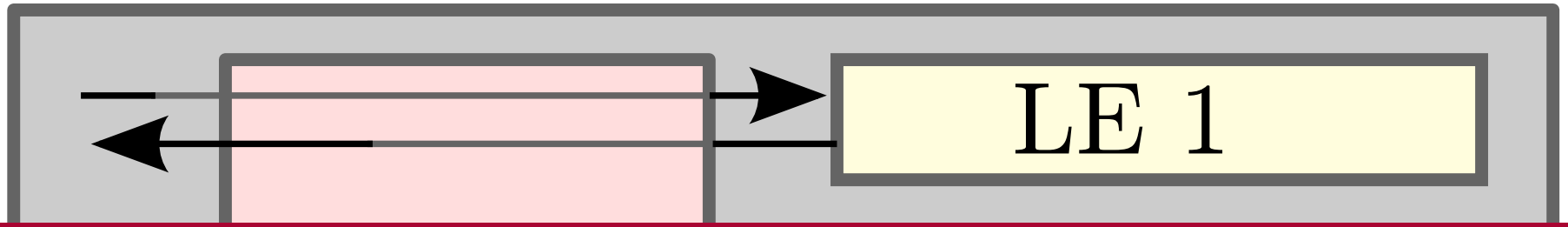


Logic Element

- 4-LUT (A, B, C, D)
- Optional Output Register





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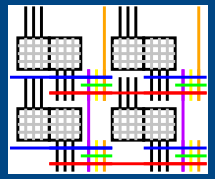
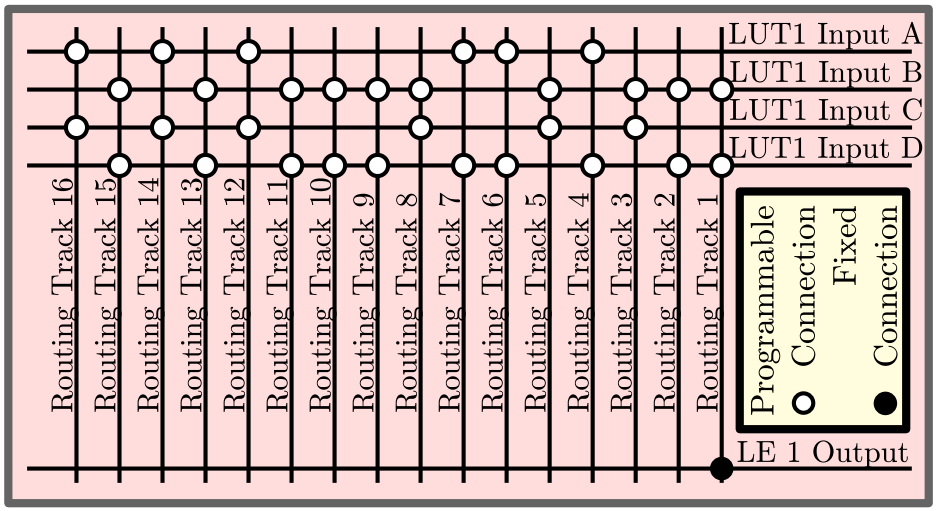


Internal Interconnect

- Connects output of LE to input of other LEs
- 50% depopulated connections



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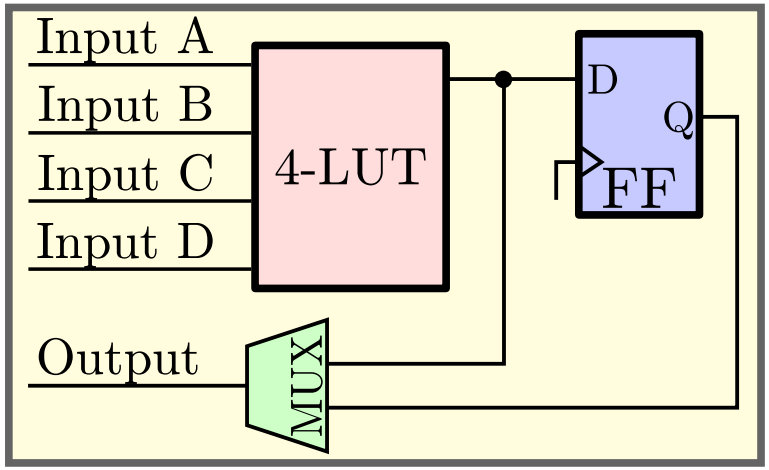

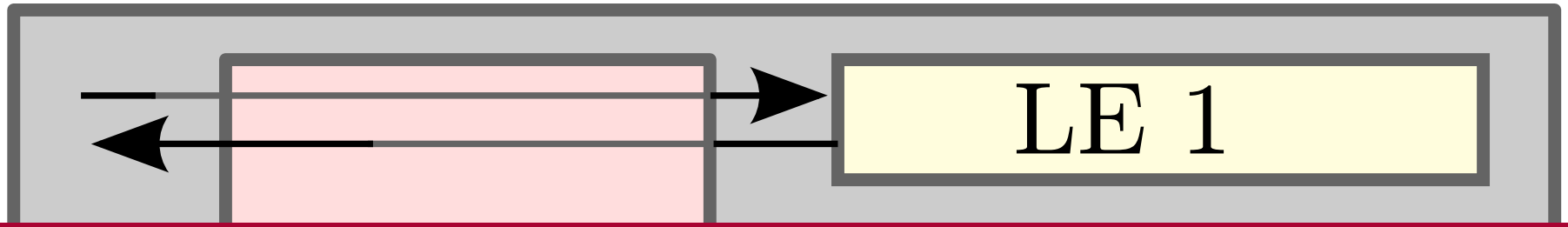

Measurable Components

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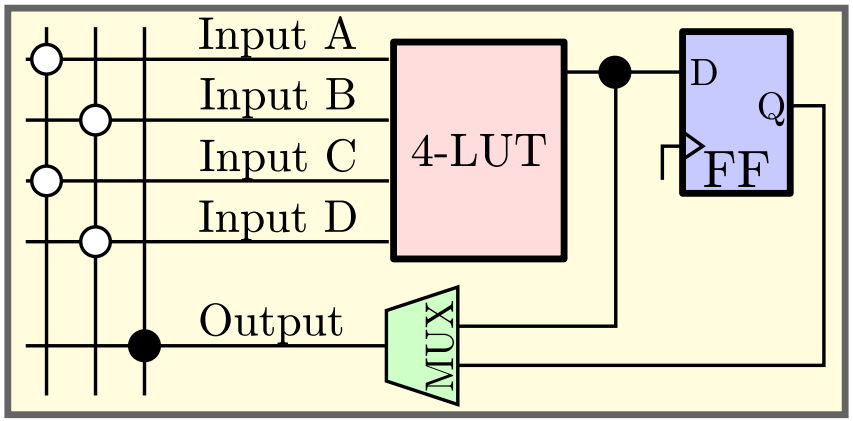

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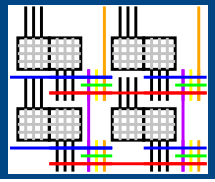
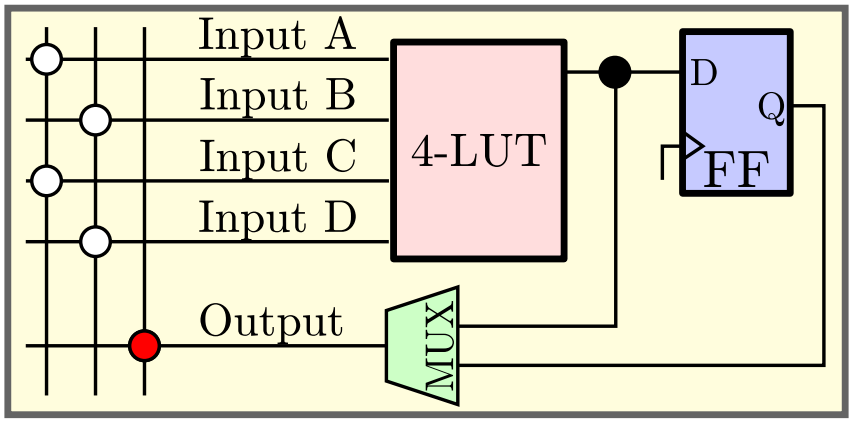


- Cannot measure individual components
- E.g., Measure crosspoint



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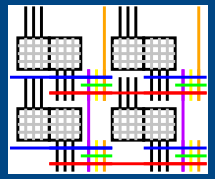

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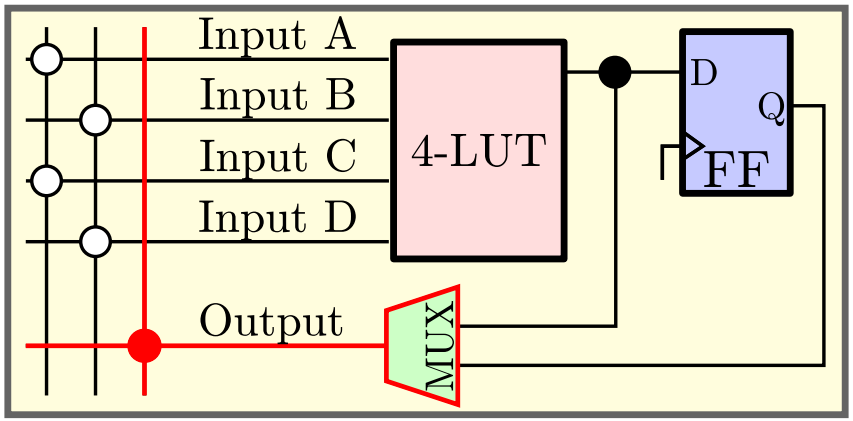
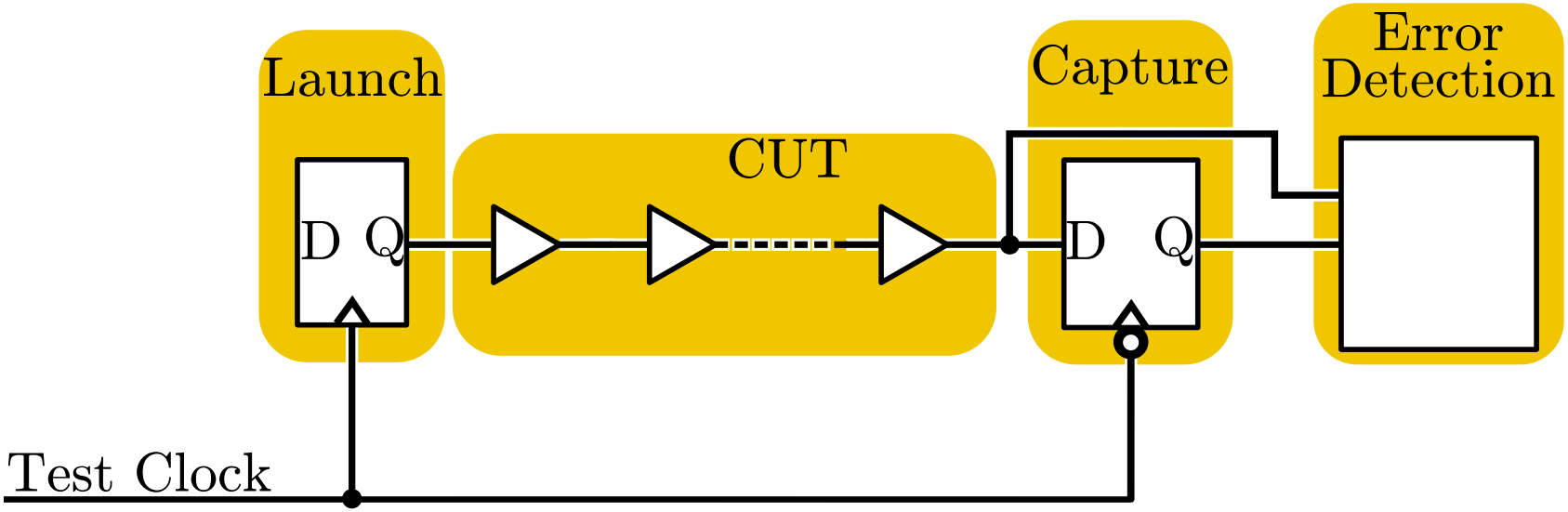
- E.g., Measure crosspoint
- Cannot differentiate from other components



- Measure groups of components

Measurable Path

- Can measure path delays between two registers
- Test for signal propagation between registers
- Sweep frequency to test for delay between registers
  - Delay includes registers



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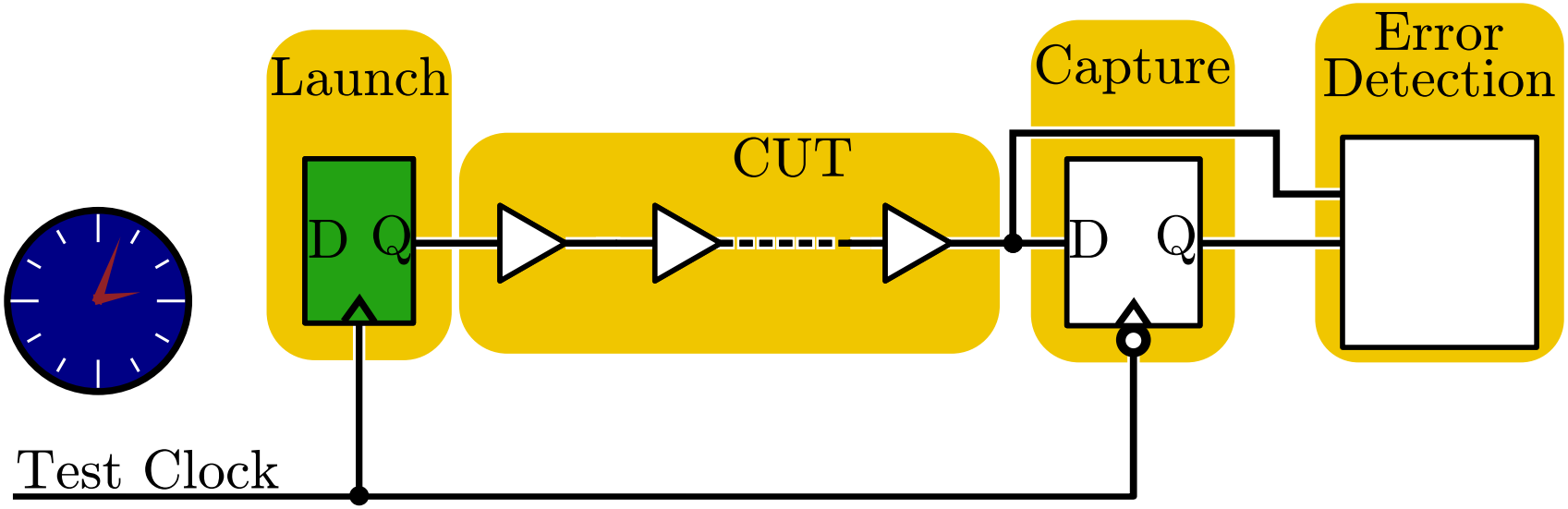

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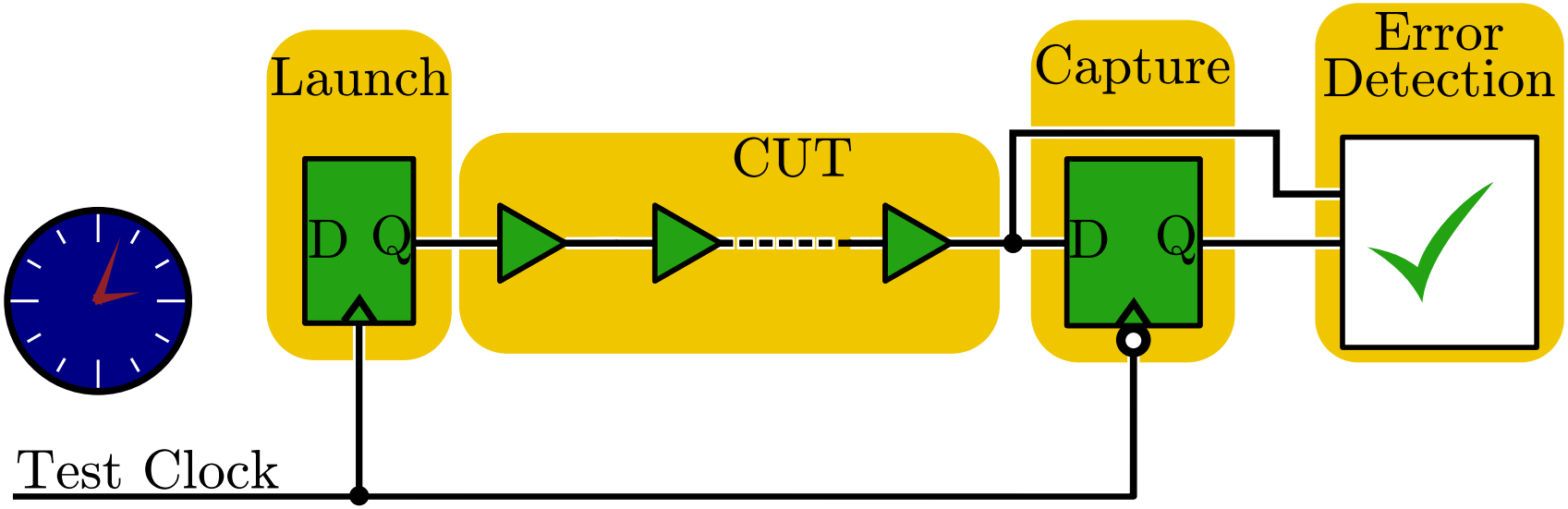

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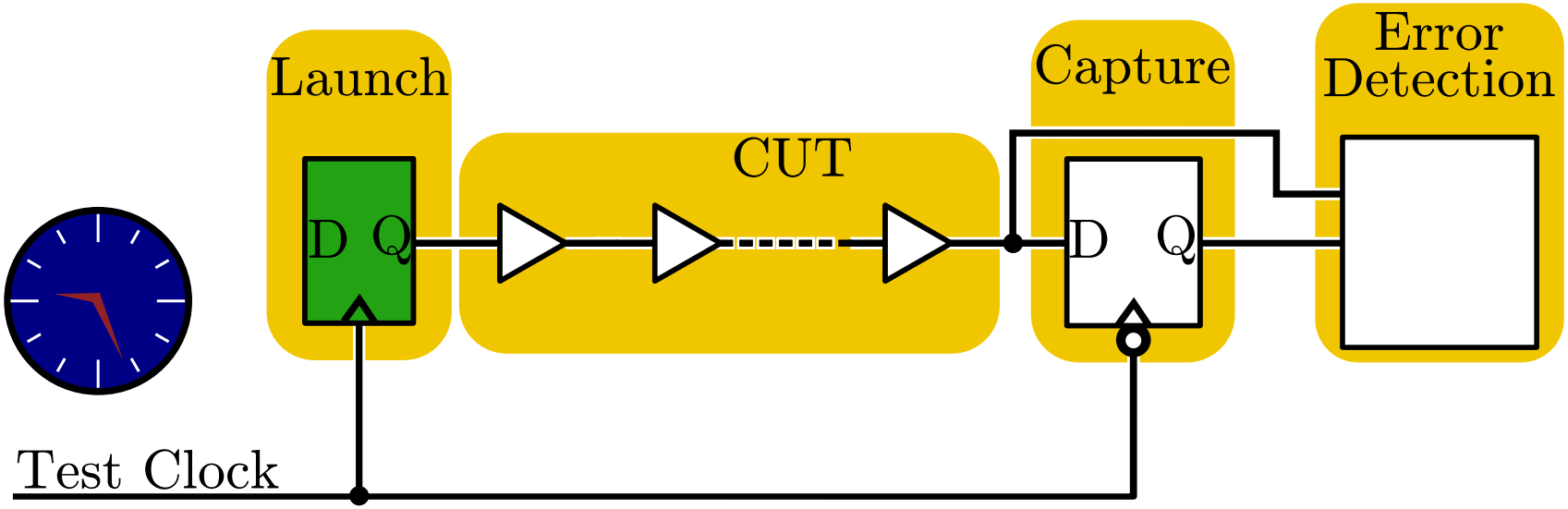

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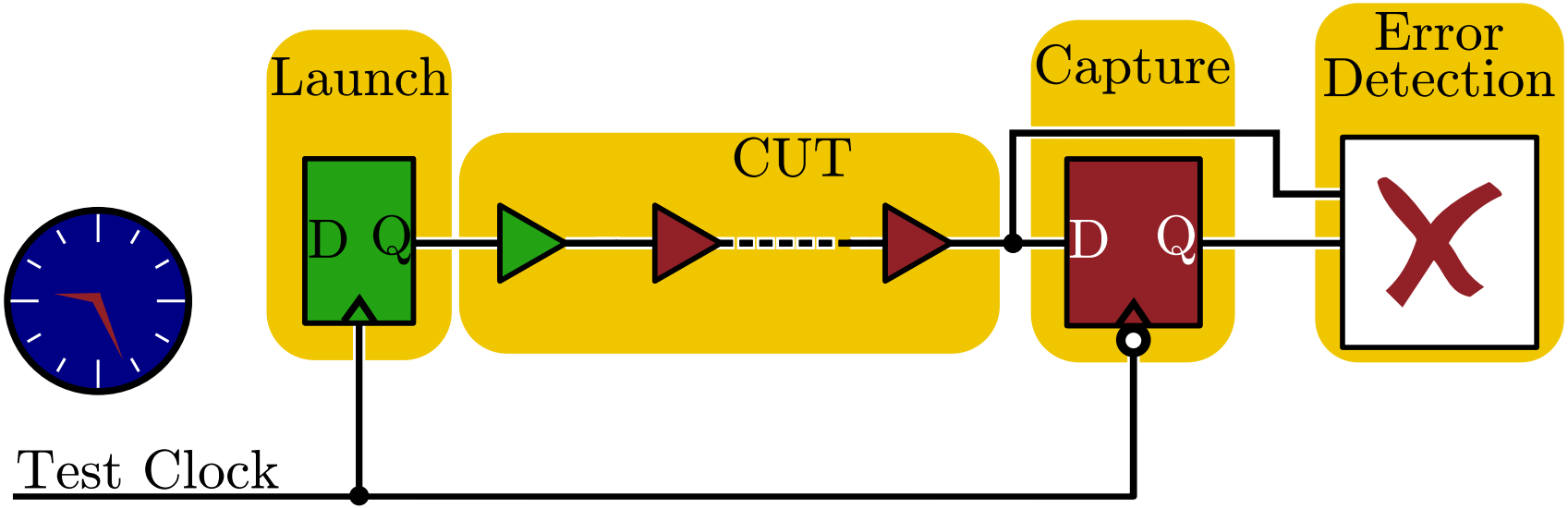
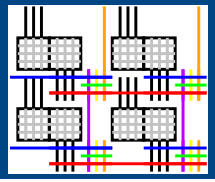


Logical Component Nodes



- Measured paths must start and end at registers
- Components must be grouped into measurable units

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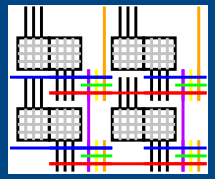

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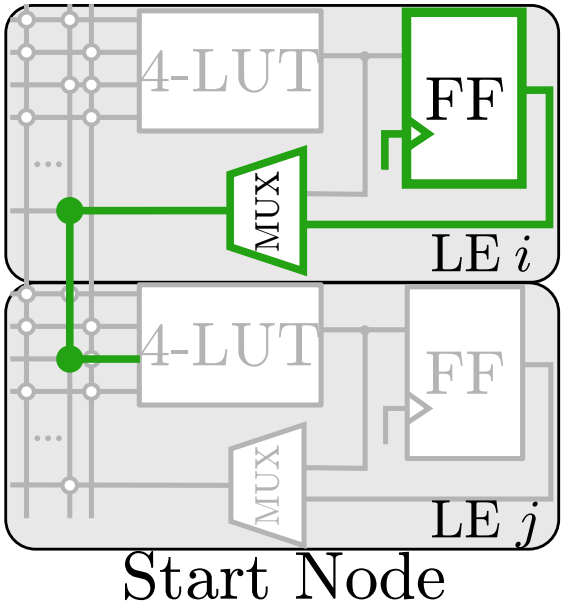

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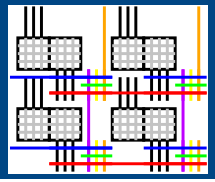

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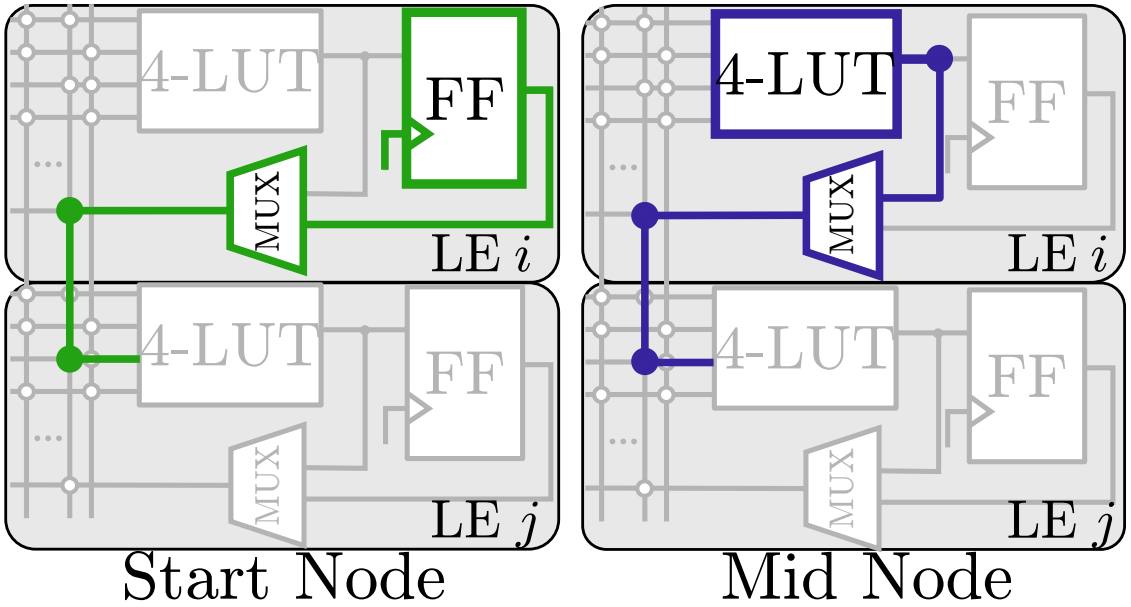

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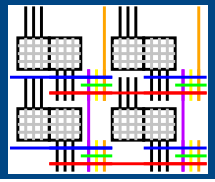

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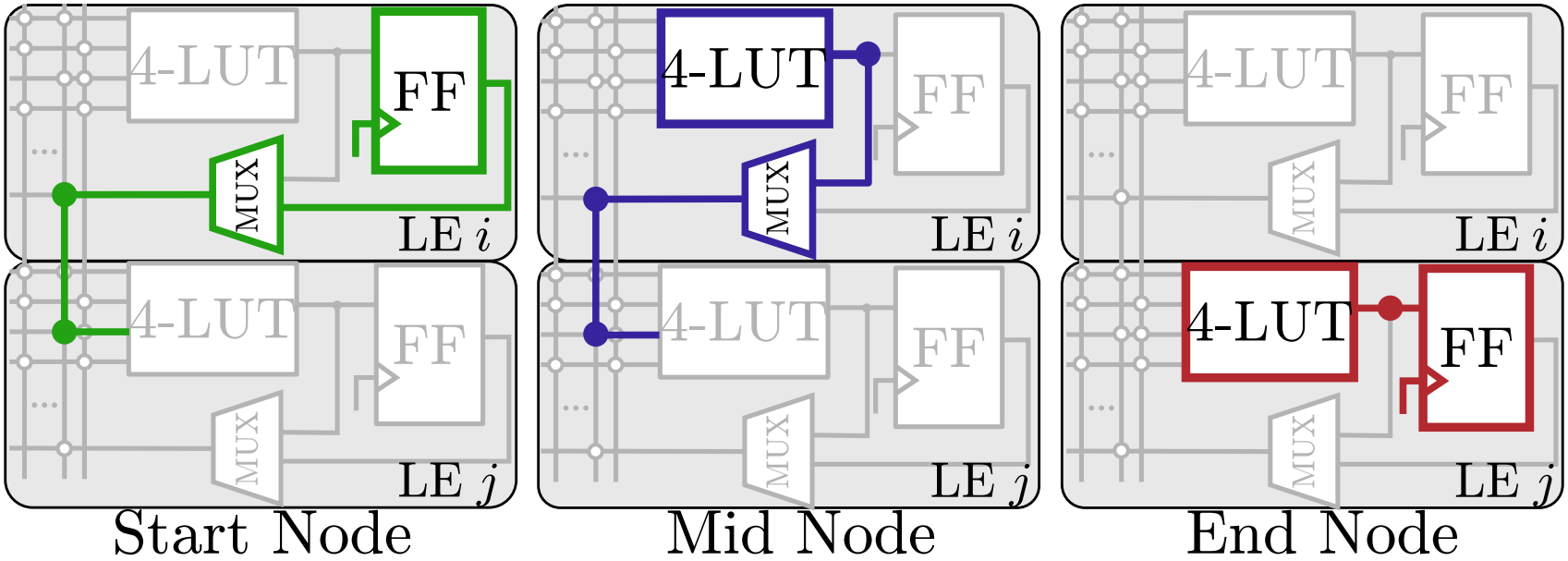

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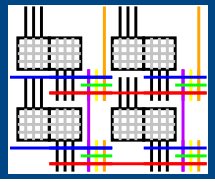

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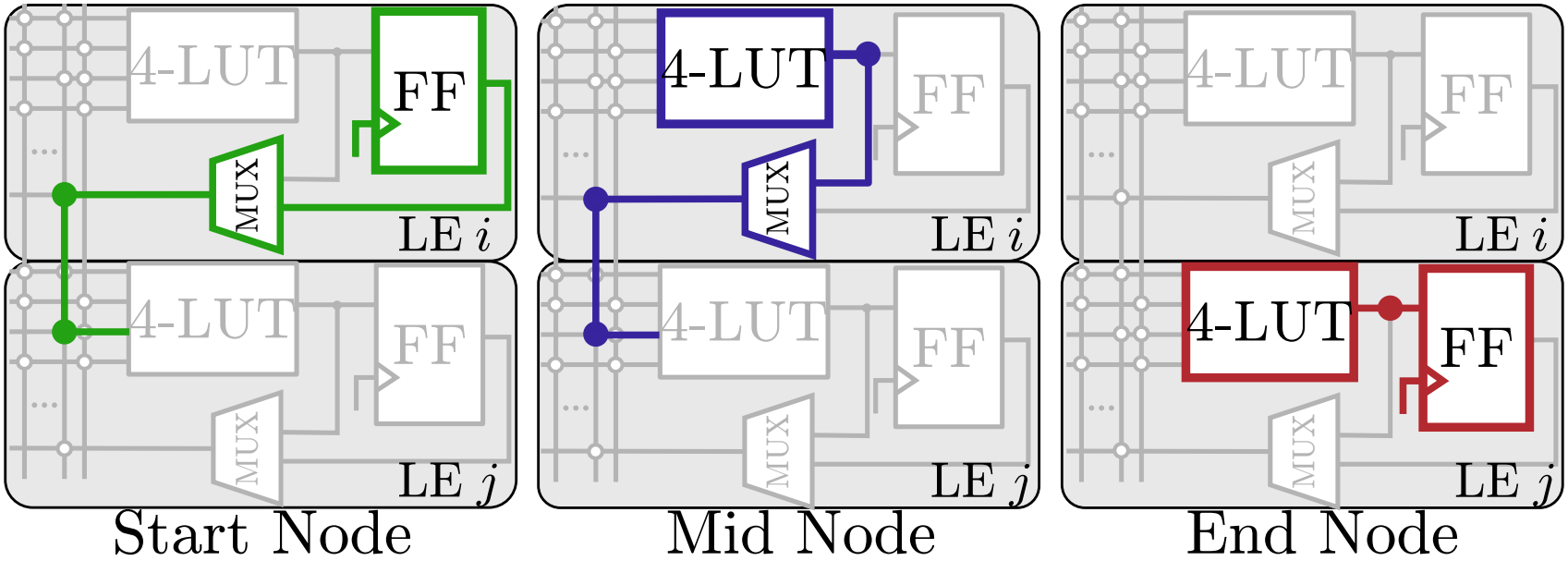
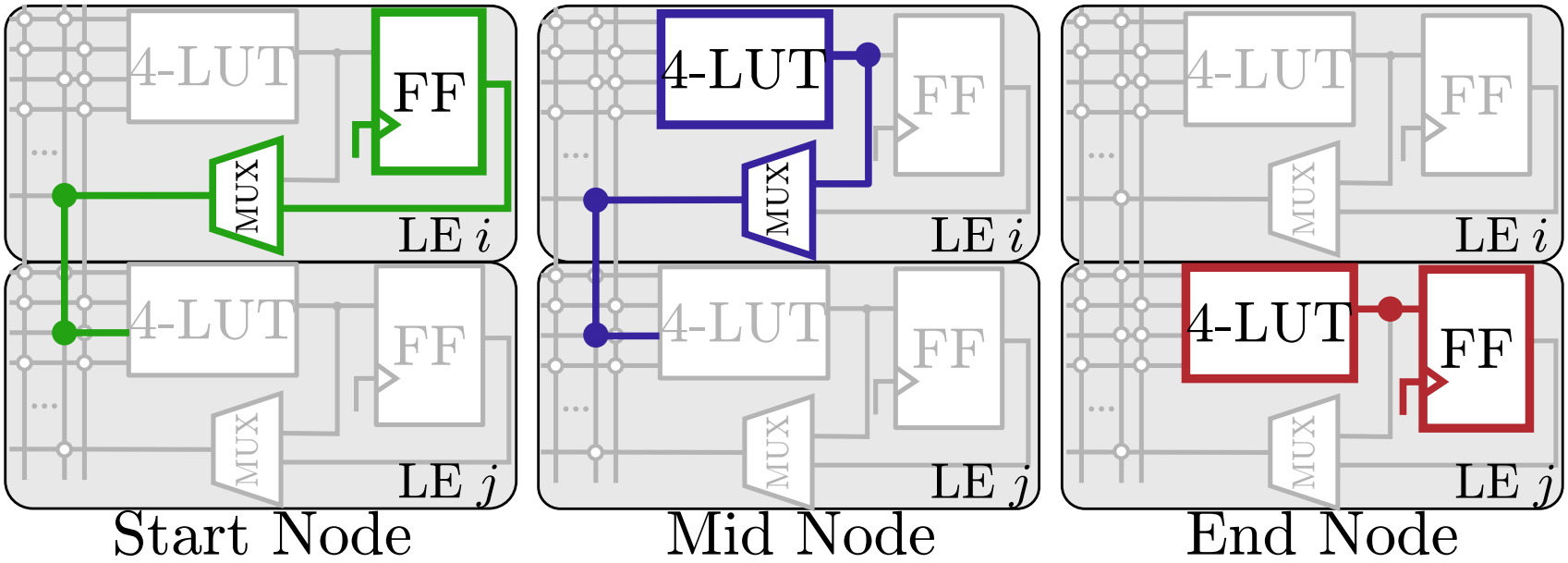


- Paths begin at Start Node, go through some Mid Nodes and stop at End Node

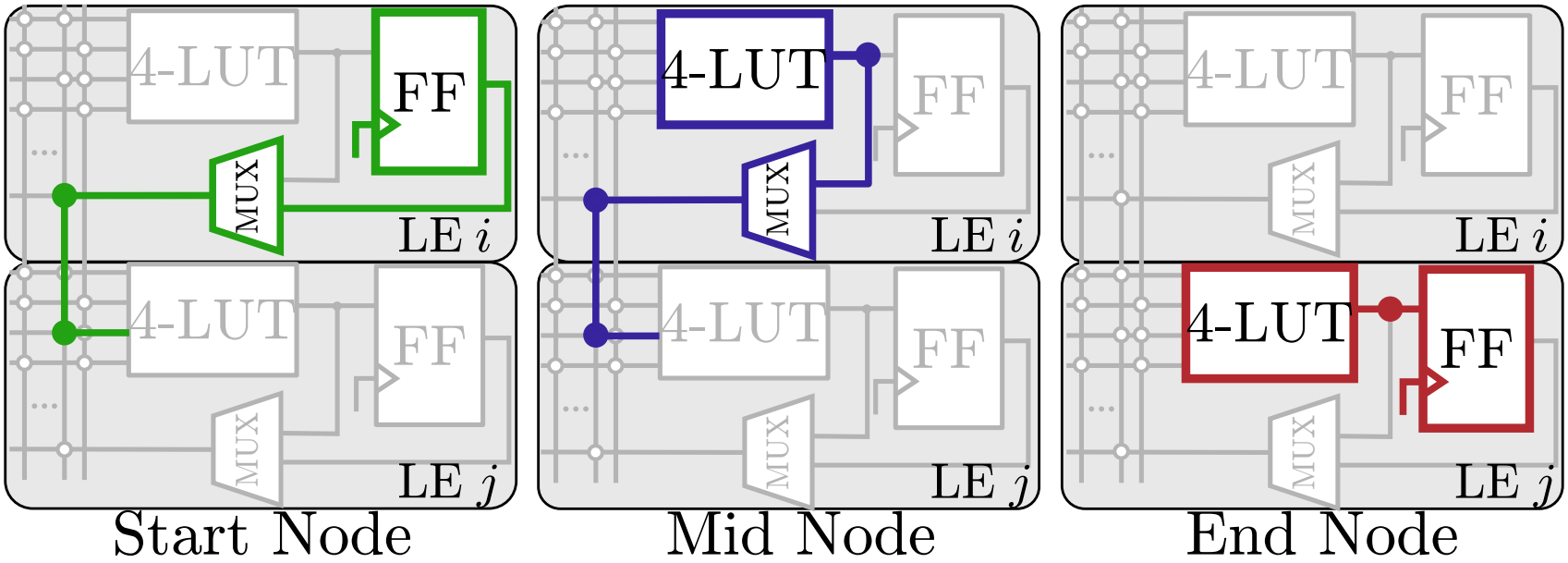
Logical Component Nodes



$16 \times 15 \times 2$

480 Nodes

Logical Component Nodes



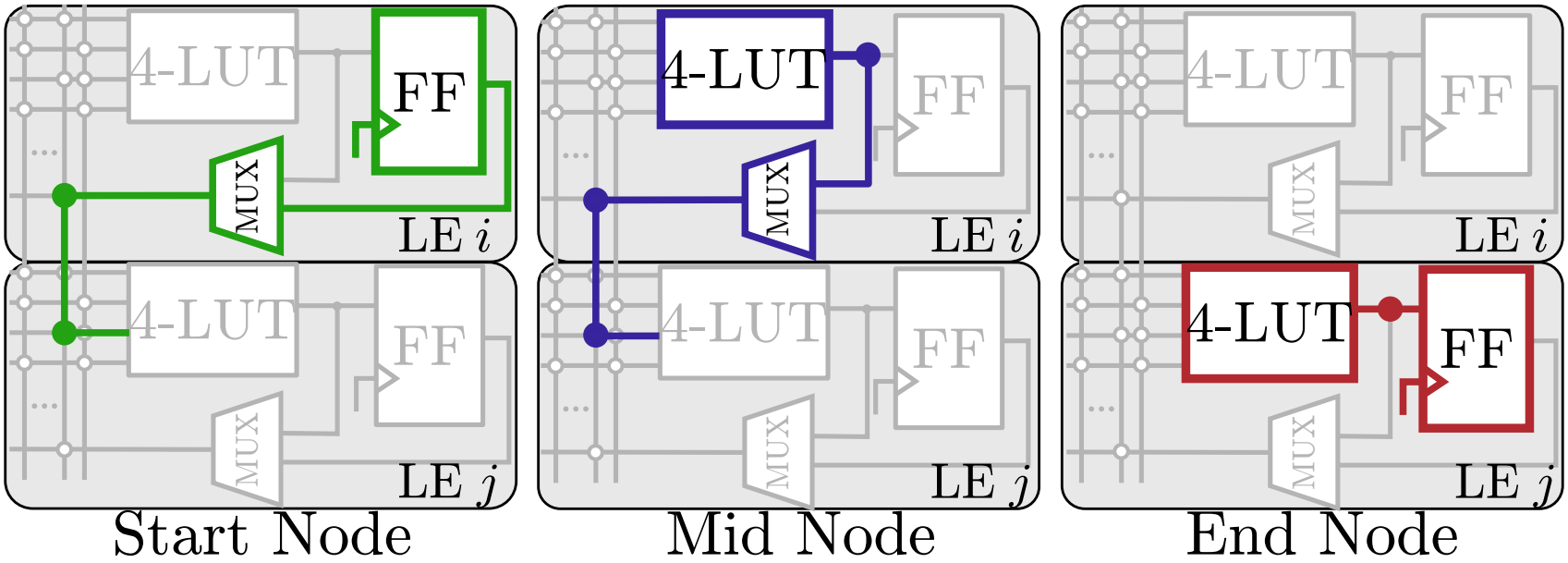
$16 \times 15 \times 2$

480 Nodes

$16 \times 15 \times 2$

480 Nodes

Logical Component Nodes



$16 \times 15 \times 2$

480 Nodes

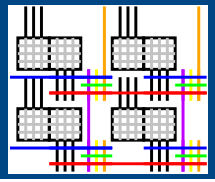
$16 \times 15 \times 2$

480 Nodes

16 Nodes

$$480 + 480 + 16 = 976 \text{ LC Nodes}$$

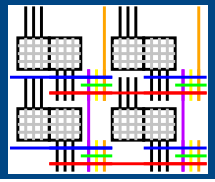
Matrix Representation



- 976 Nodes in one LAB $\rightarrow$ measure at least 976 paths
- Represent as path-node matrix

	S_1	S_2	S_3	M_1	M_2	M_3	M_4	E_1	E_2	E_3
Path 1	1	0	0	1	0	1	0	1	0	0
Path 2	0	1	0	0	1	0	1	1	0	0
Path 3	0	0	1	0	0	1	1	0	0	1
Path 4	1	0	0	0	1	0	0	0	1	0
	Start Nodes			Mid Nodes				End Nodes		

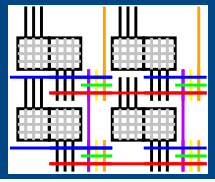
Matrix Representation



- 976 Nodes in one LAB $\rightarrow$ measure at least 976 paths
- Represent as path-node matrix
- Augment with path delay and solve

	S_1	S_2	S_3	M_1	M_2	M_3	M_4	E_1	E_2	E_3	
Path 1	1	0	0	1	0	1	0	1	0	0	3.7
Path 2	0	1	0	0	1	0	1	1	0	0	3.5
Path 3	0	0	1	0	0	1	1	0	0	1	4.2
Path 4	1	0	0	0	1	0	0	0	1	0	2.3
	Start Nodes			Mid Nodes				End Nodes			Path Delays

Matrix Representation



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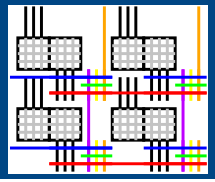
Path 4	1	0	0	0	1	0	0	0	1	0	2.3
	Start Nodes			Mid Nodes				End Nodes			Path Delays

- $\approx 10^{18}$ paths in one LAB.
- Complete path-node Matrix 976×10^{18}

Matrix Representation



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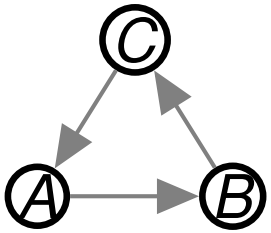
Path 1	1	0	0	1	0	1	0	1	0	0	3.7
Path 2	0	1	0	0	1	0	1	1	0	0	3.5
Path 3	0	0	1	0	0	1	1	0	0	1	4.2
Path 4	1	0	0	0	1	0	0	0	1	0	2.3
	Start Nodes			Mid Nodes				End Nodes			Path Delays

- $\approx 10^{18}$ paths in one LAB.
- Complete path-node Matrix 976×10^{18}
- Complete path-node Matrix has rank of only 960
  - Cannot solve for all LC Nodes $\rightarrow$ Short by 16
  - Generally true when using Launch-Capture technique

Reconsider Measurable Component

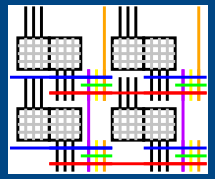
- Cannot solve for LC Nodes
- Redefine measurable component



Discrete Unit of Knowledge (DUK)

Small linear combination of LC Nodes

Reconsider Measurable Component

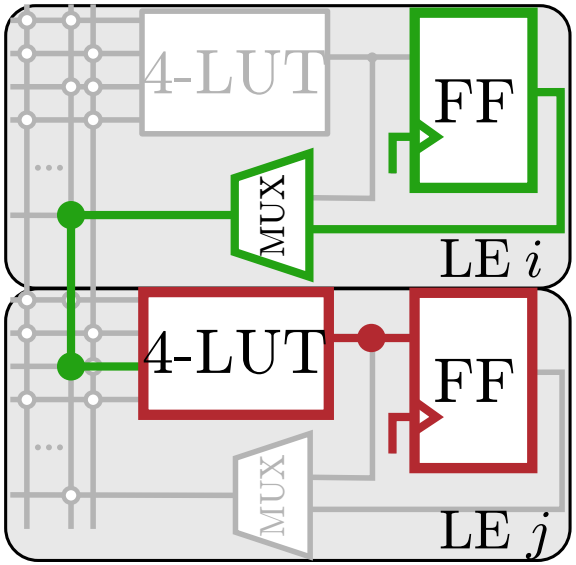


- Cannot solve for LC Nodes
- Redefine measurable component

Discrete Unit of Knowledge (DUK)

Small linear combination of LC Nodes

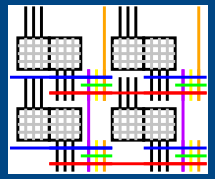
Mother DUK



$${}_iS_j + {}_jE = {}_iMD_j$$

480 M-DUKs

Reconsider Measurable Component



- Cannot solve for LC Nodes
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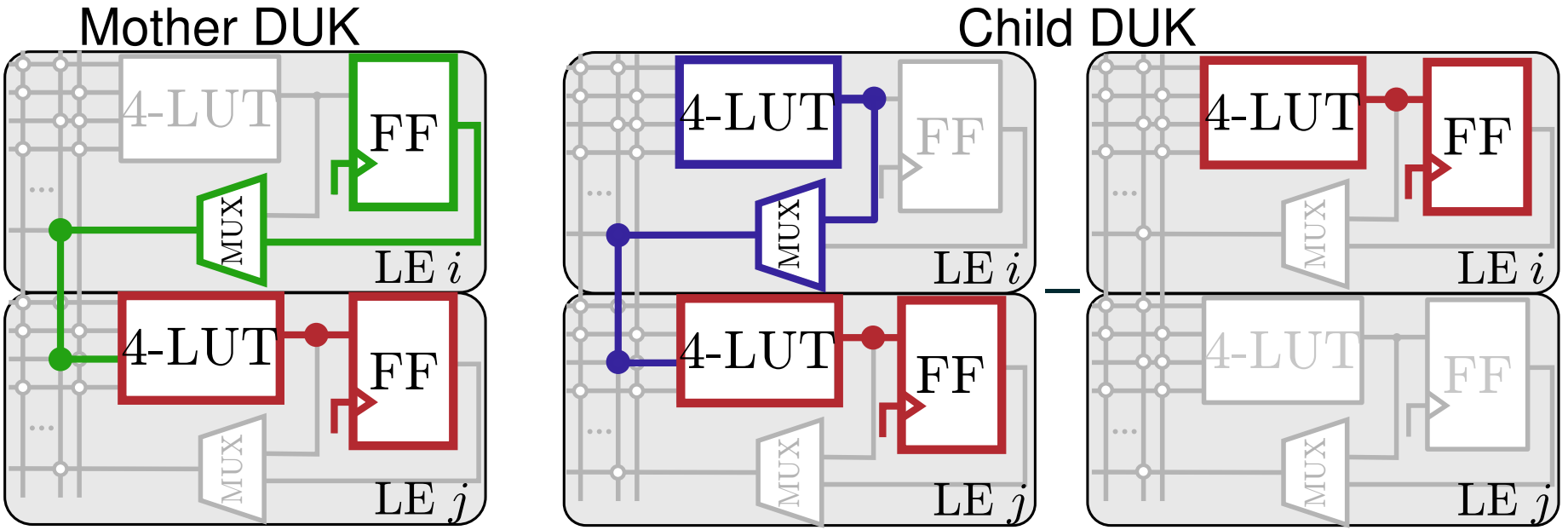
Discrete Unit of Knowledge (DUK)

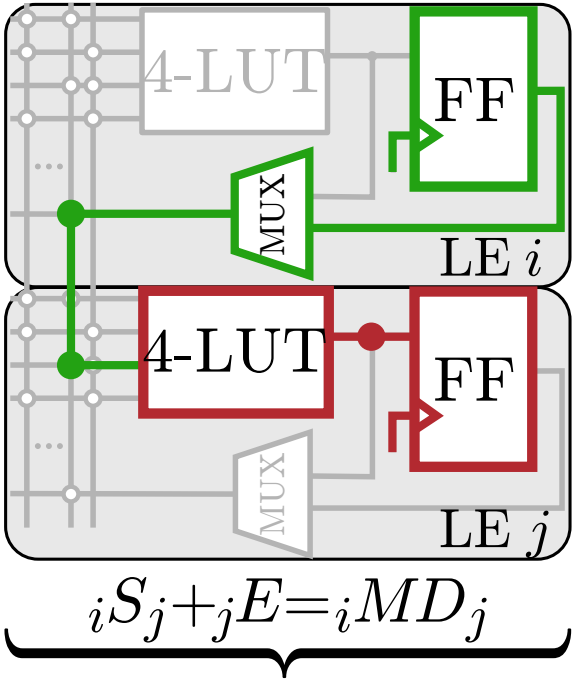
Small linear combination of LC Nodes



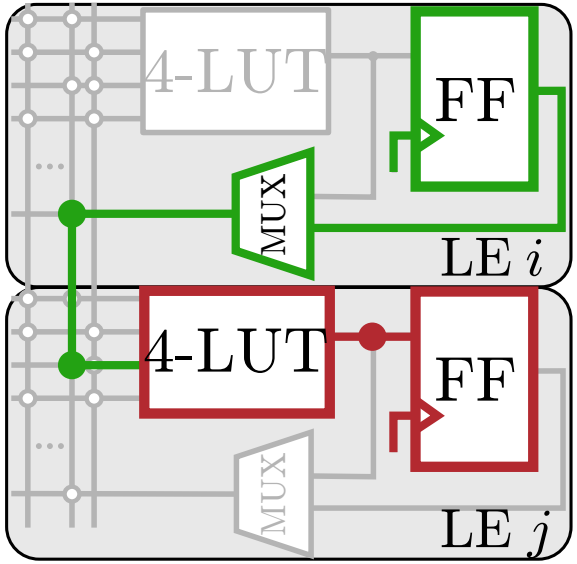
480 M-DUKs

480 C-DUKs

DUK - LC Node Equivalence



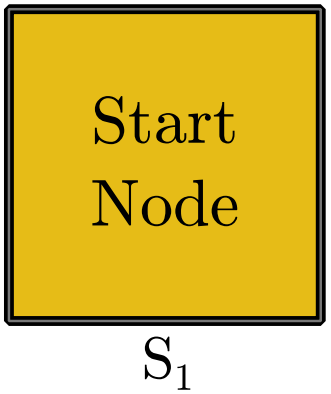
DUK - LC Node Equivalence



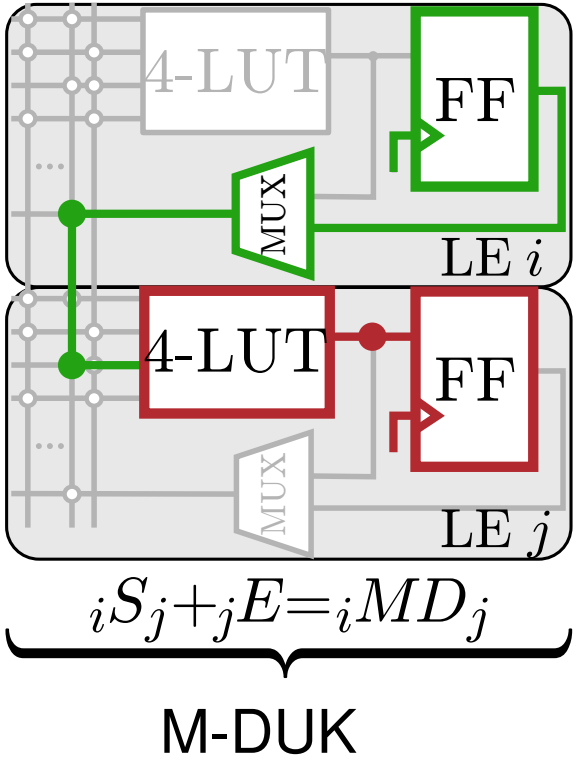
$${}_iS_j + {}_jE = {}_iMD_j$$

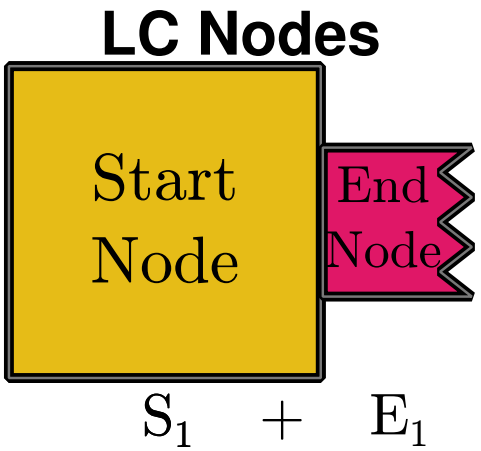
M-DUK

LC Nodes

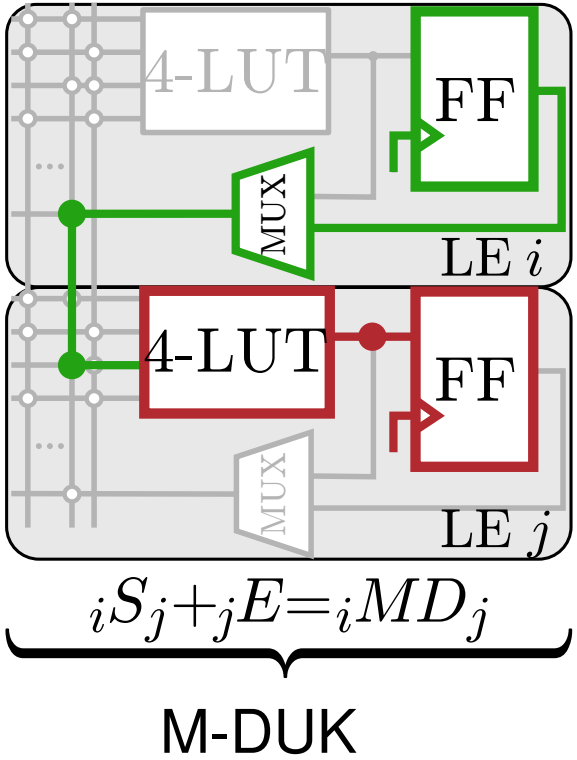


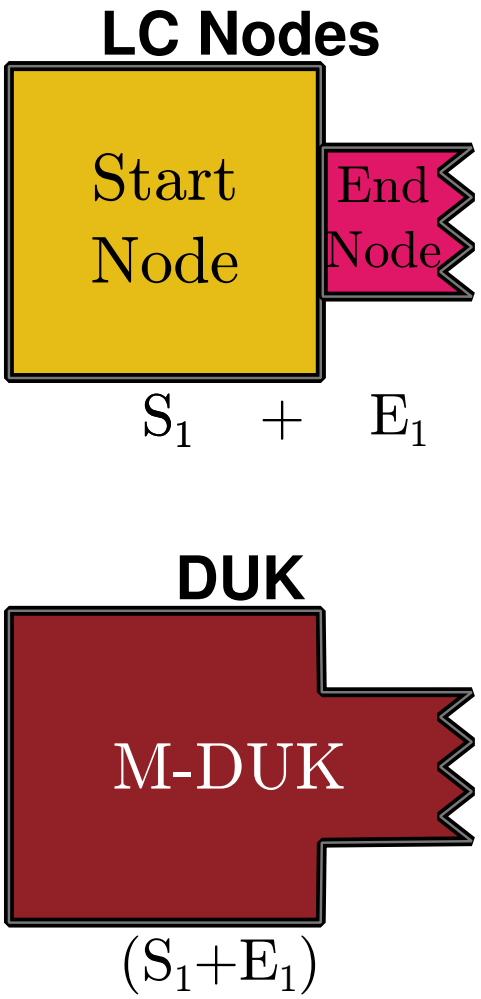
DUK - LC Node Equivalence



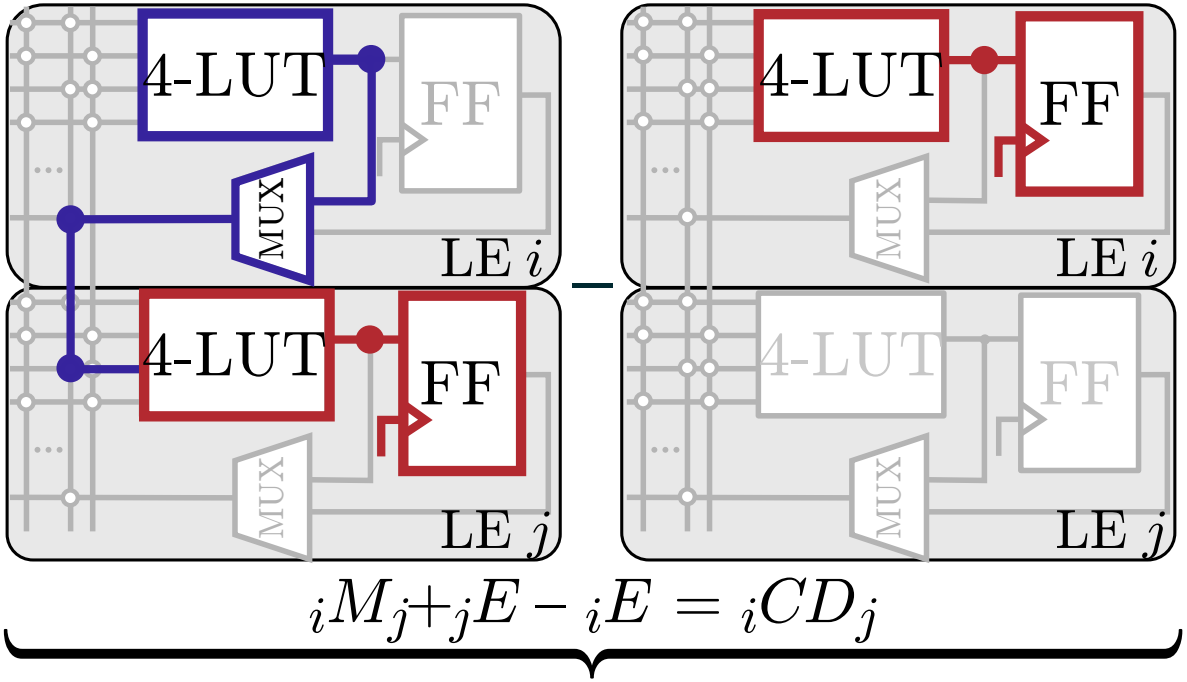


DUK - LC Node Equivalence



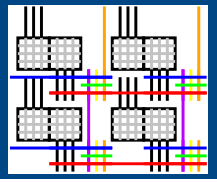


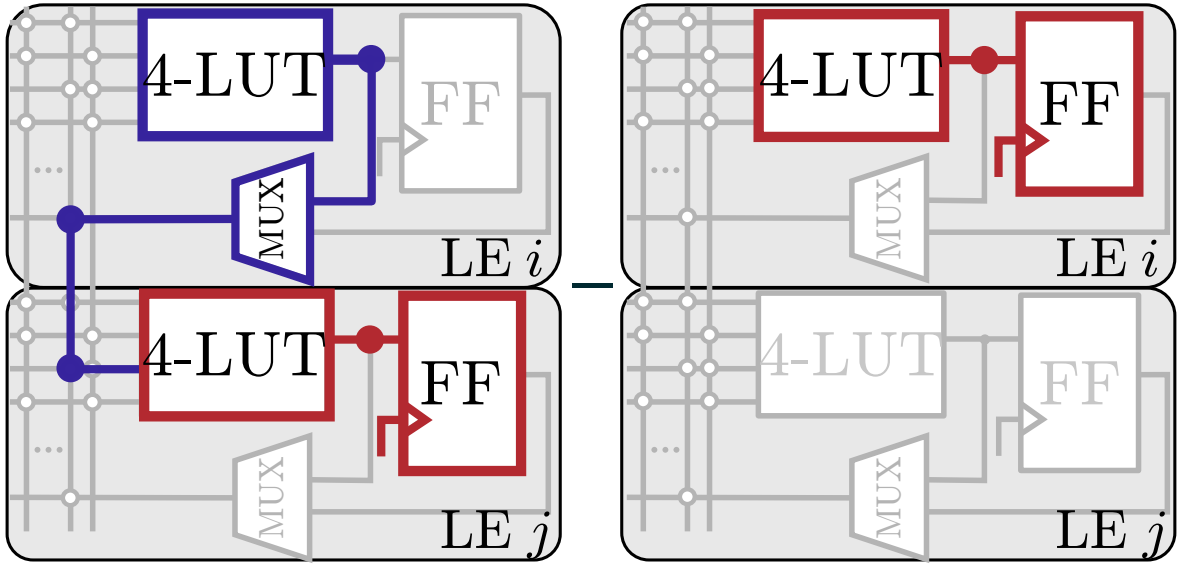
DUK - LC Node Equivalence



$$\underbrace{{}_iM_j + {}_jE - {}_iE = {}_iCD_j}_{\text{C-DUK}}$$

DUK - LC Node Equivalence





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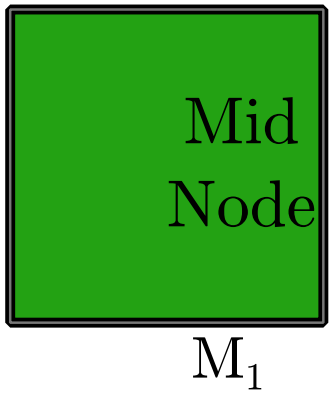
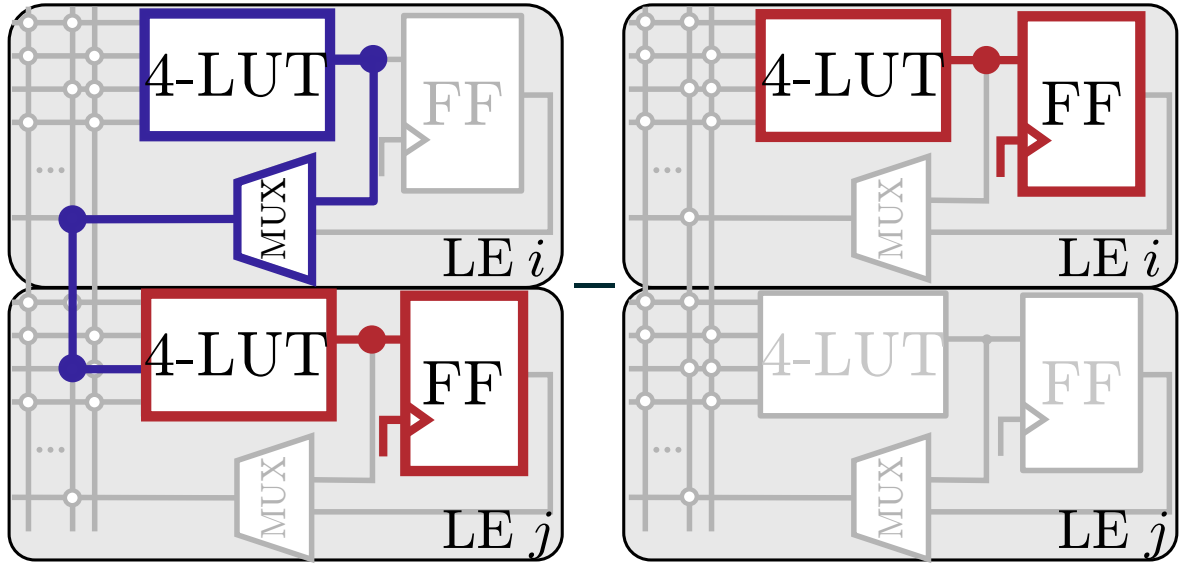
LC Nodes



DUK - LC Node Equivalence



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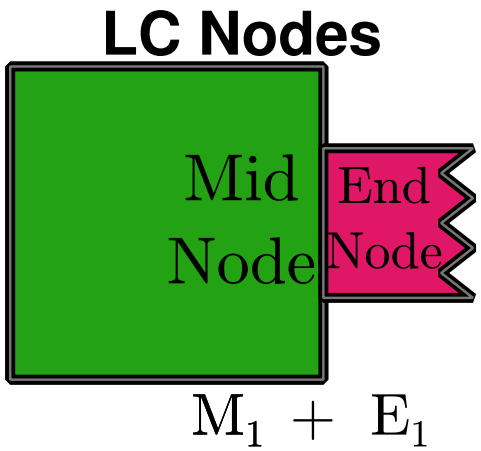

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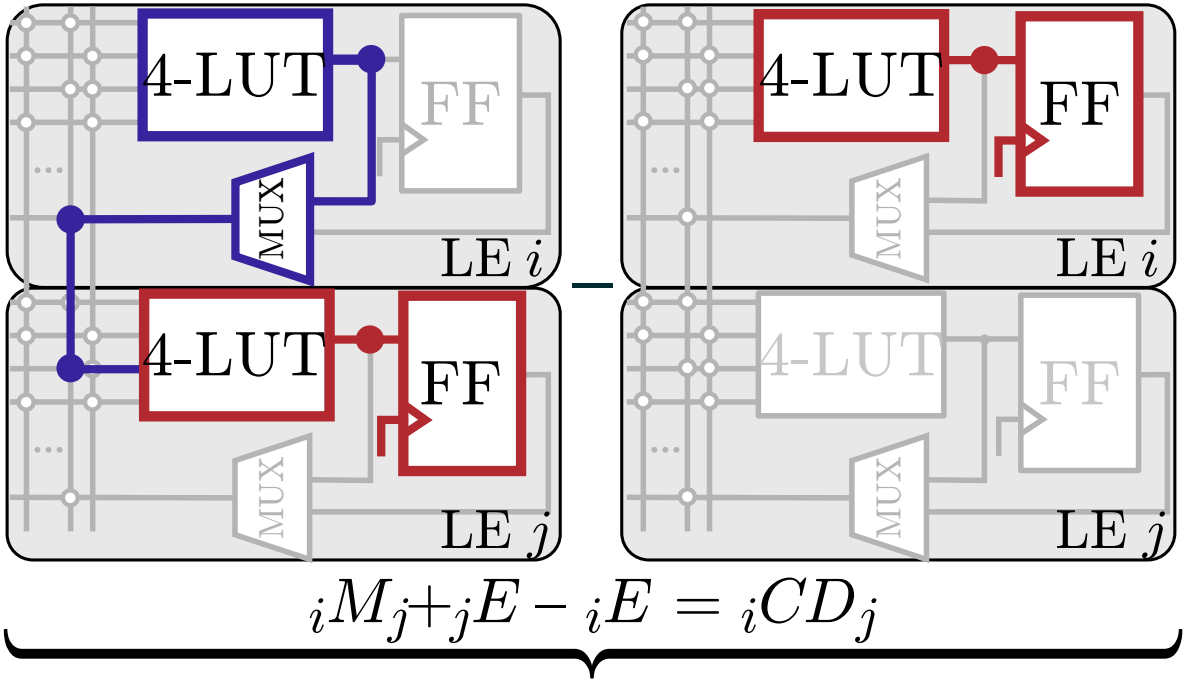
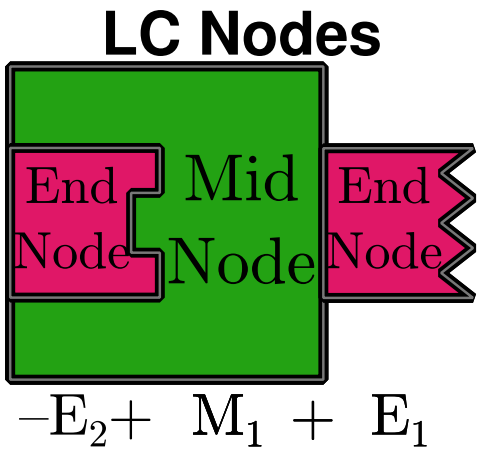
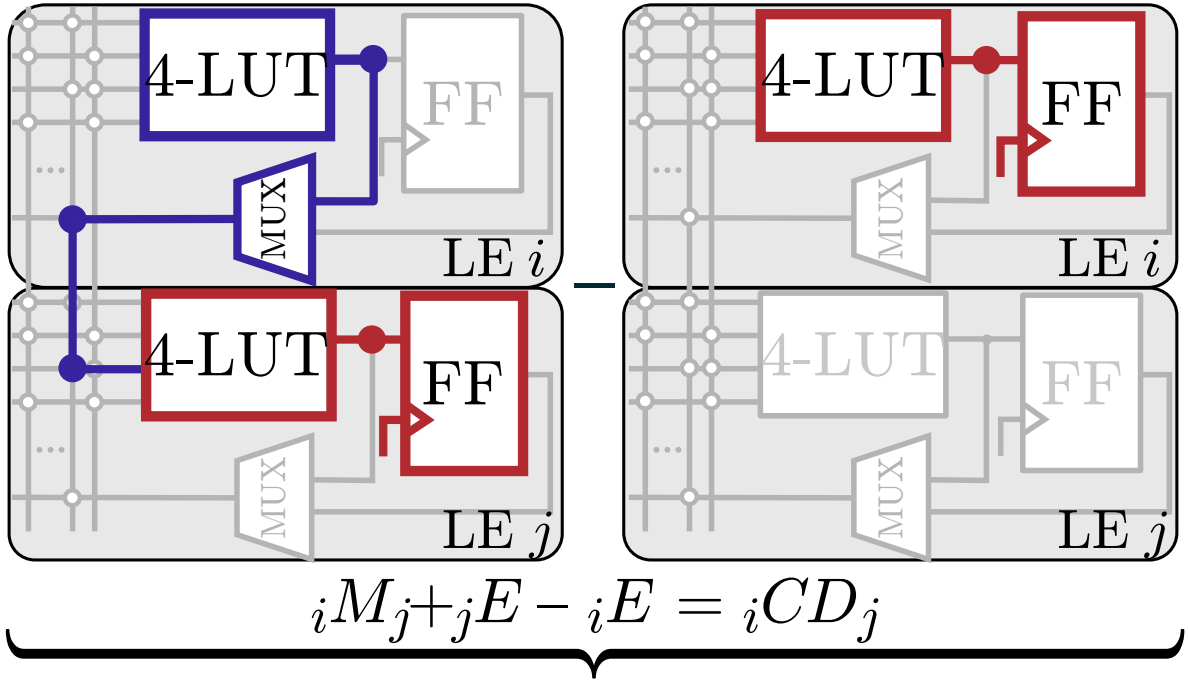
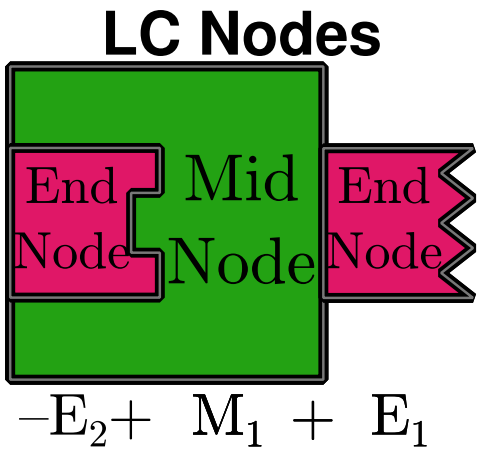
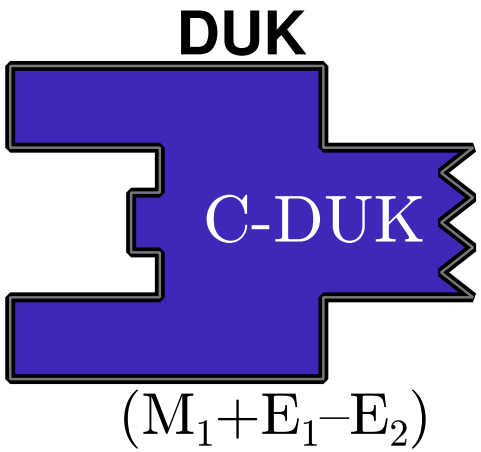




DUK - LC Node Equivalence





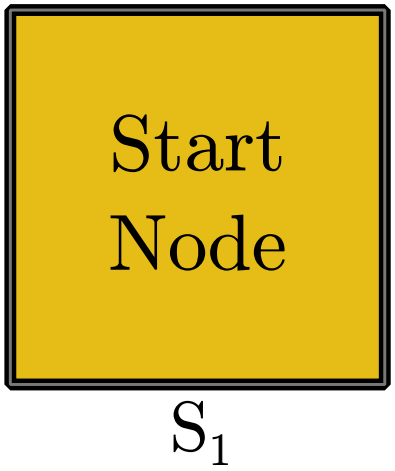


DUK - LC Node Equivalence

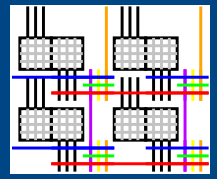
LC Node-based paths $\Leftrightarrow$ DUK-based paths

DUK - LC Node Equivalence

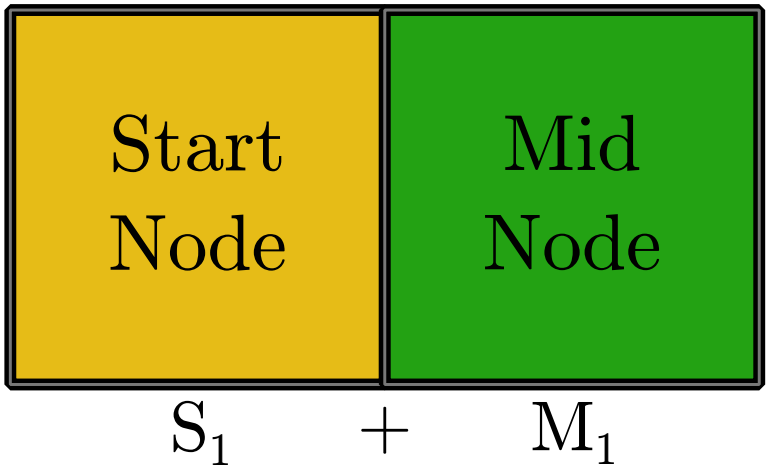
LC Node-based paths $\Leftrightarrow$ DUK-based paths



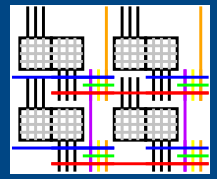
DUK - LC Node Equivalence



LC Node-based paths $\Leftrightarrow$ DUK-based paths



DUK - LC Node Equivalence



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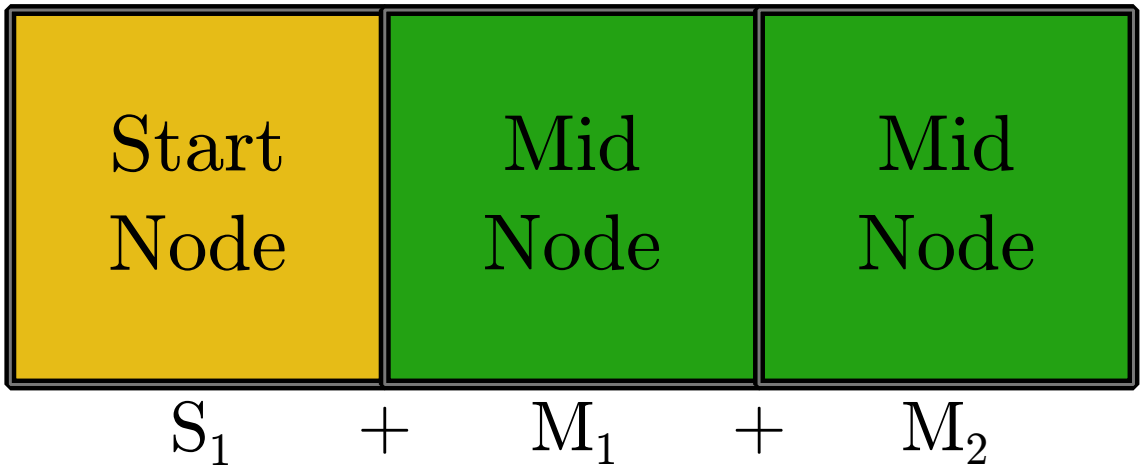

DUK - LC Node Equivalence

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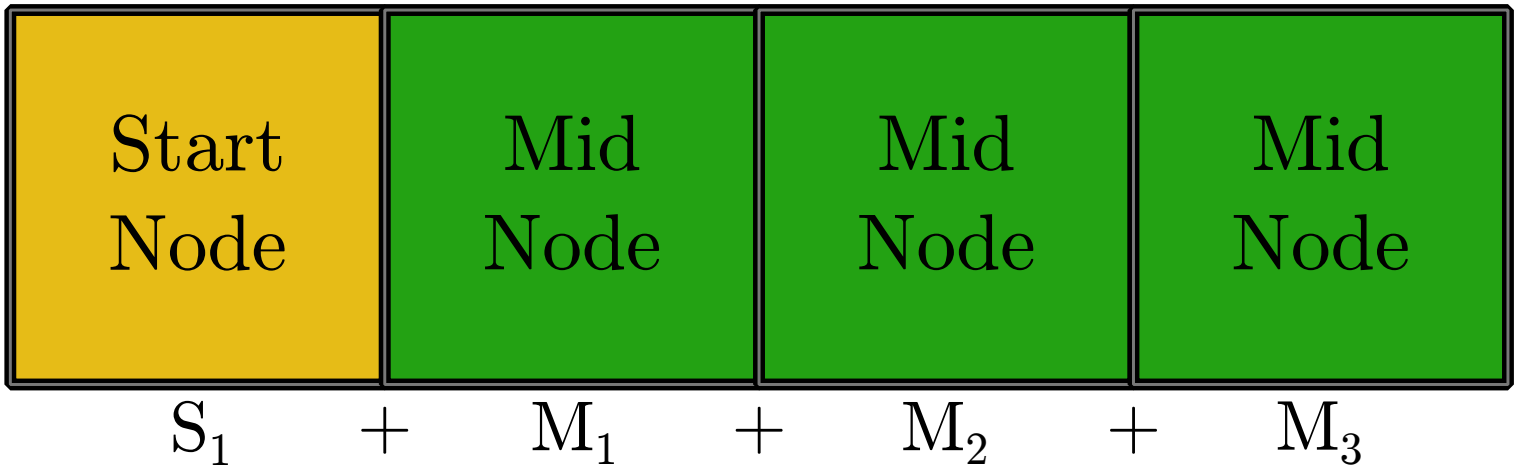

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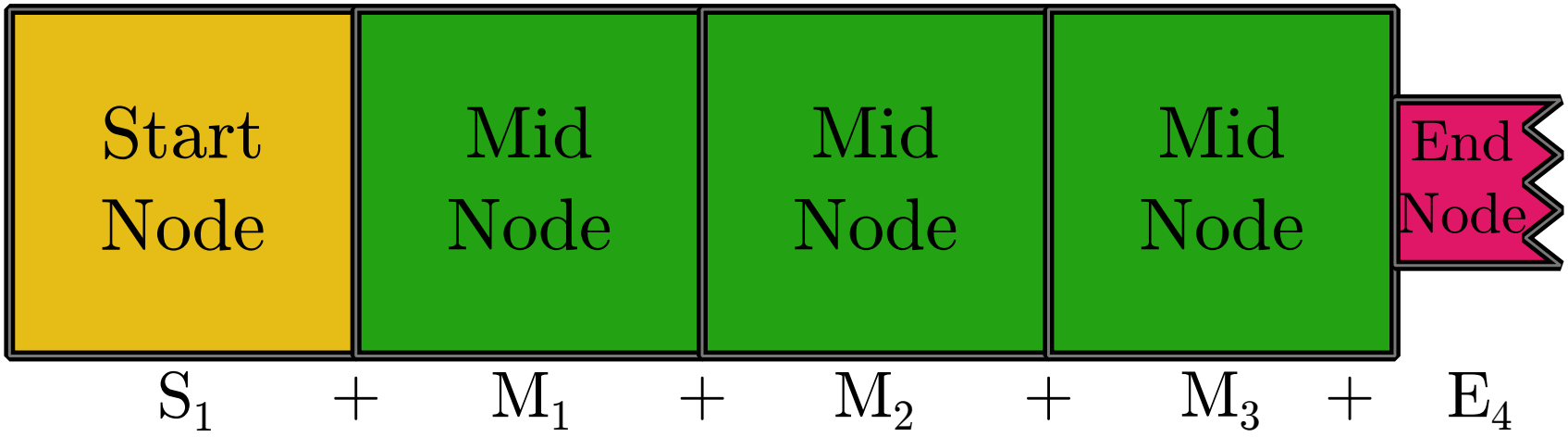
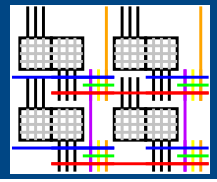
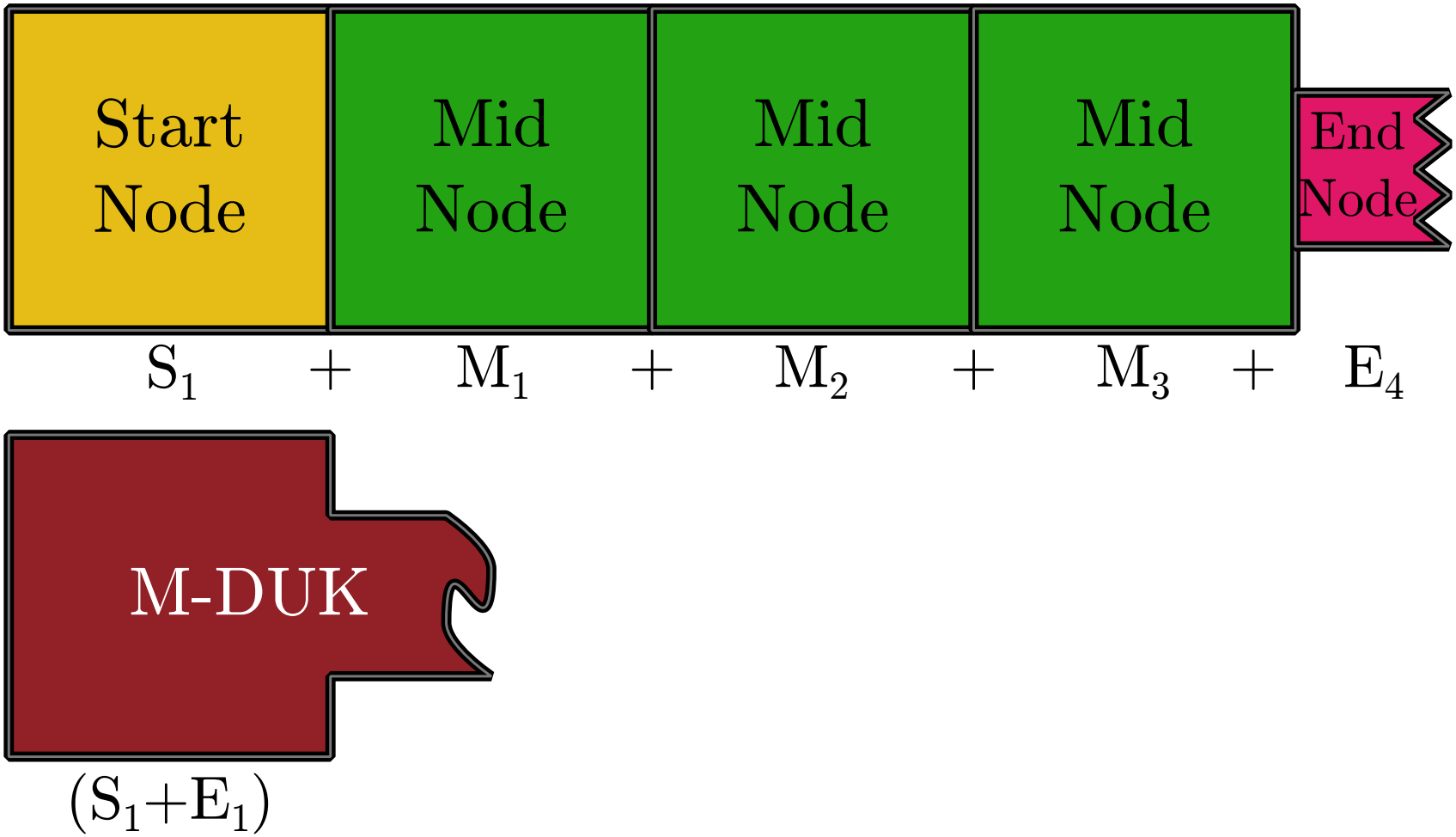


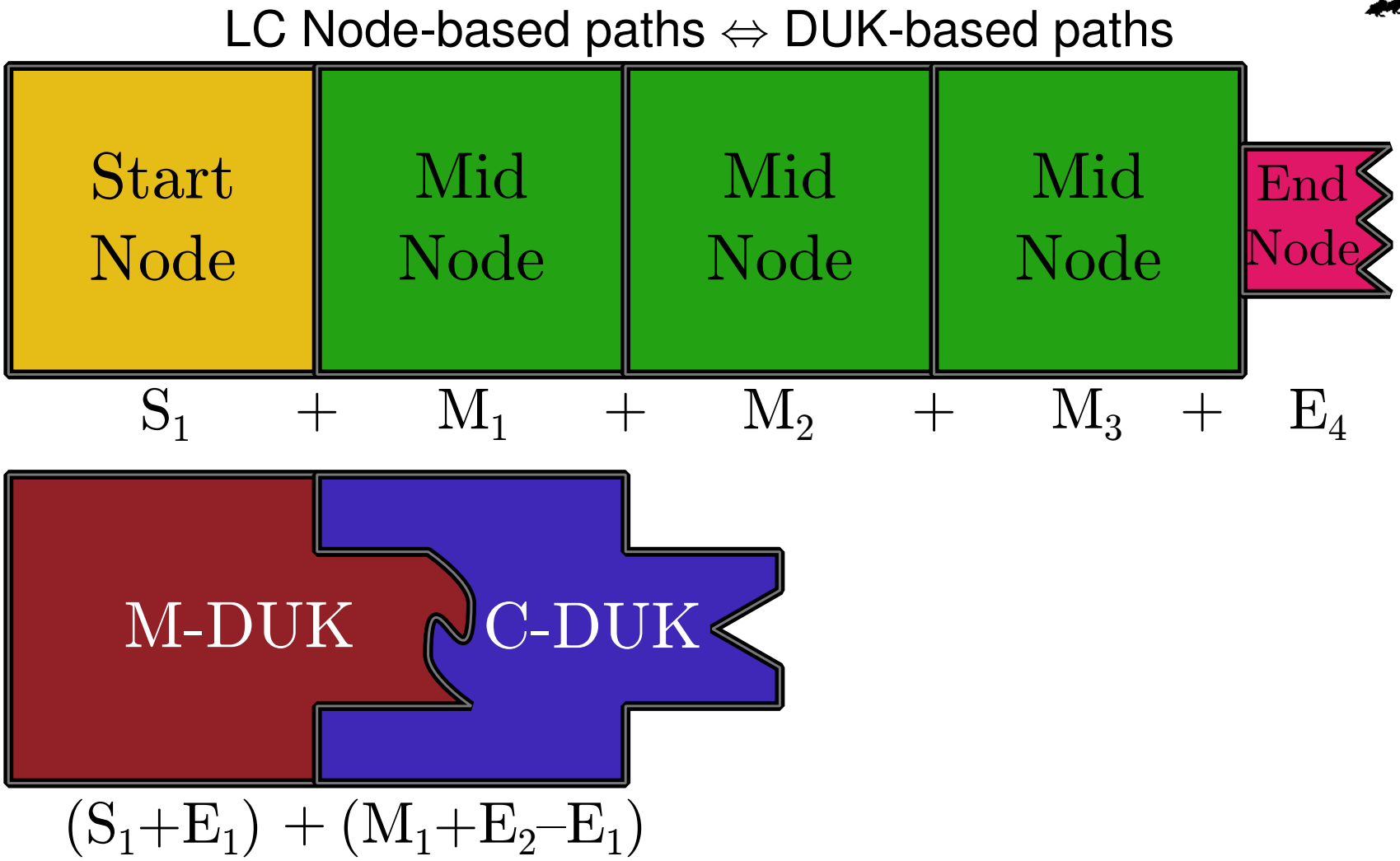
DUK - LC Node Equivalence



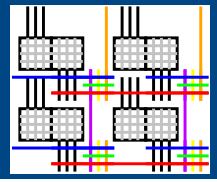
LC Node-based paths ⇔ DUK-based paths



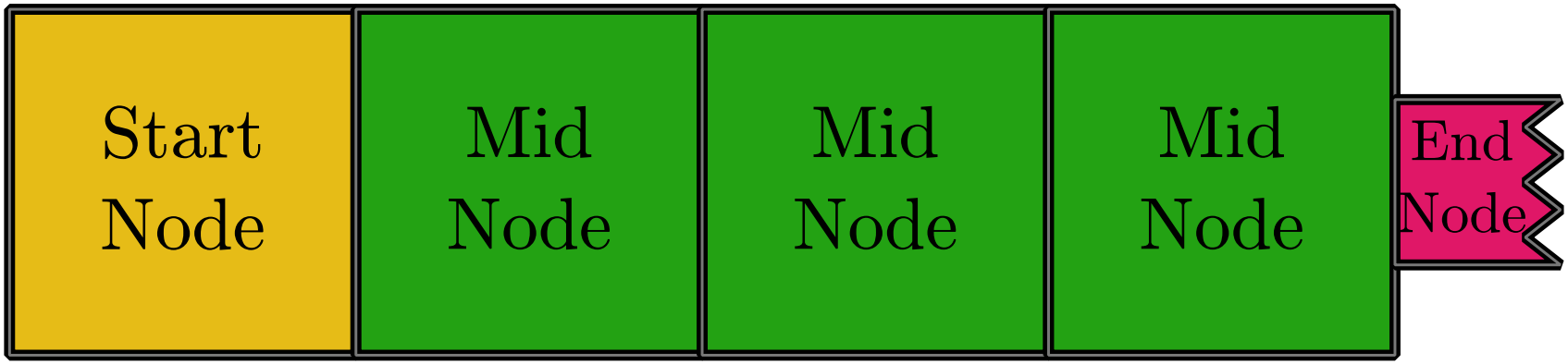
DUK - LC Node Equivalence



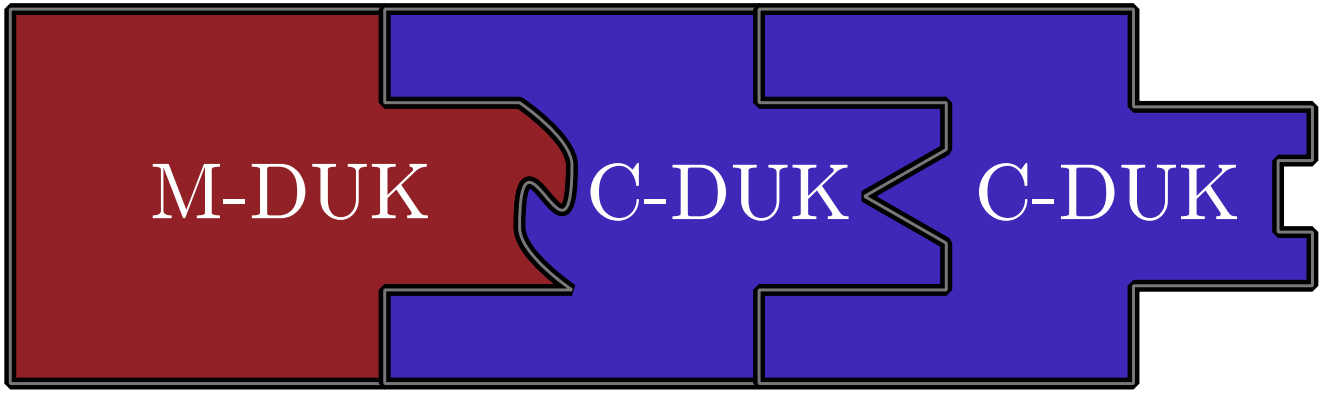
DUK - LC Node Equivalence



LC Node-based paths ⇔ DUK-based paths

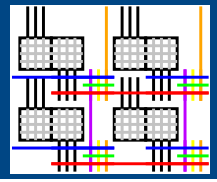


$$S_1 + M_1 + M_2 + M_3 + E_4$$

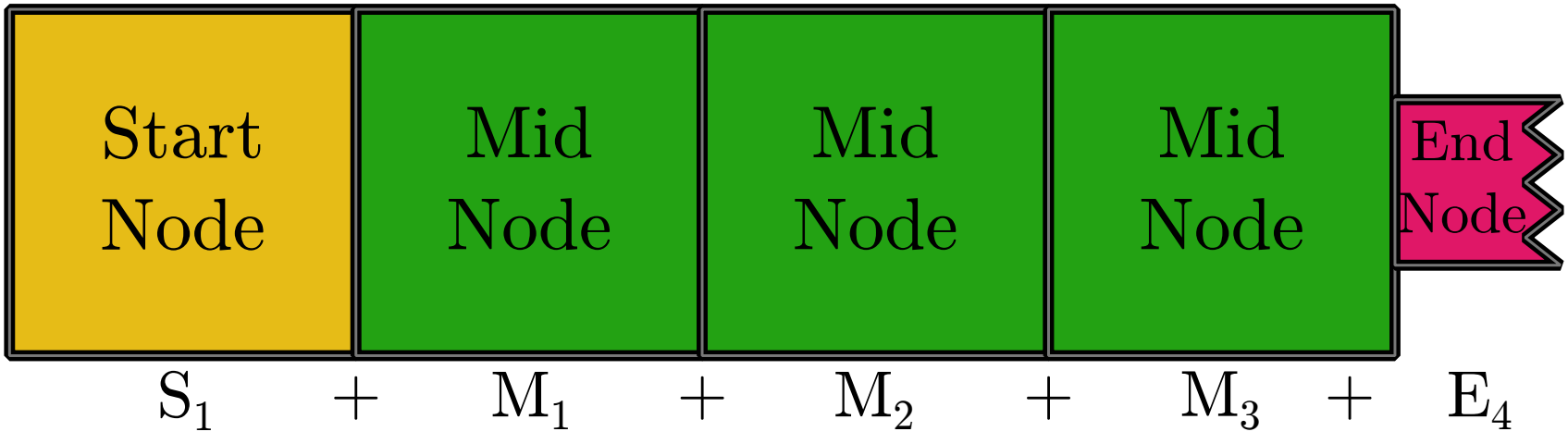


$$(S_1+E_1) + (M_1+E_2-E_1)+(M_2+E_3-E_2)$$

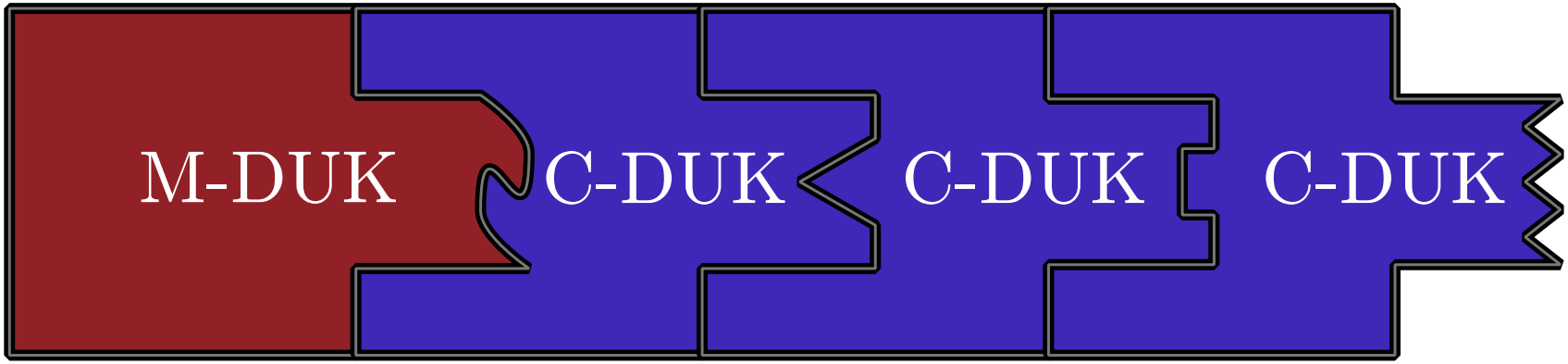
DUK - LC Node Equivalence



LC Node-based paths ⇔ DUK-based paths



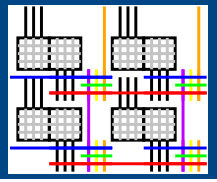
$$S_1 + M_1 + M_2 + M_3 + E_4$$



$$(S_1+E_1) + (M_1+E_2-E_1)+(M_2+E_3-E_2)+(M_3+E_4-E_3)$$

- Paths begin at M-DUK, go through zero or more C-DUKs

Matrix Representation – DUKs

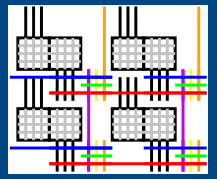


- 960 DUKs $\rightarrow$ measure at least 960 paths.
- Represent as path-DUK matrix

	M_1	M_2	M_3	C_1	C_2	C_3	C_4
Path 1	1	0	0	1	0	1	0
Path 2	0	1	0	0	1	0	1
Path 3	0	0	1	0	0	1	1
Path 4	1	0	0	0	1	0	0

M-DUKs C-DUKs

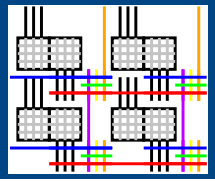
Matrix Representation – DUKs



- 960 DUKs $\rightarrow$ measure at least 960 paths.
- Represent as path-DUK matrix
- Augment with path delay and solve

	M_1	M_2	M_3	C_1	C_2	C_3	C_4	
Path 1	1	0	0	1	0	1	0	3.7
Path 2	0	1	0	0	1	0	1	3.5
Path 3	0	0	1	0	0	1	1	4.2
Path 4	1	0	0	0	1	0	0	2.3
	M-DUKs			C-DUKs				Path Delays

Matrix Representation – DUKs

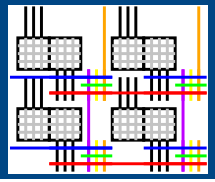


- 960 DUKs $\rightarrow$ measure at least 960 paths.
- Represent as path-DUK matrix
- Augment with path delay and solve

	M_1	M_2	M_3	C_1	C_2	C_3	C_4	
Path 1	1	0	0	1	0	1	0	3.7
Path 2	0	1	0	0	1	0	1	3.5
Path 3	0	0	1	0	0	1	1	4.2
Path 4	1	0	0	0	1	0	0	2.3
	M-DUKs			C-DUKs				Path Delays

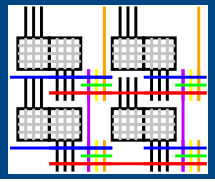
- $\approx 10^{18}$ paths in one LAB.
- Complete path-DUK Matrix 960×10^{18}
- Complete path-DUK Matrix has rank of 960
  - Can solve for all DUKs!

Which Paths to Measure?



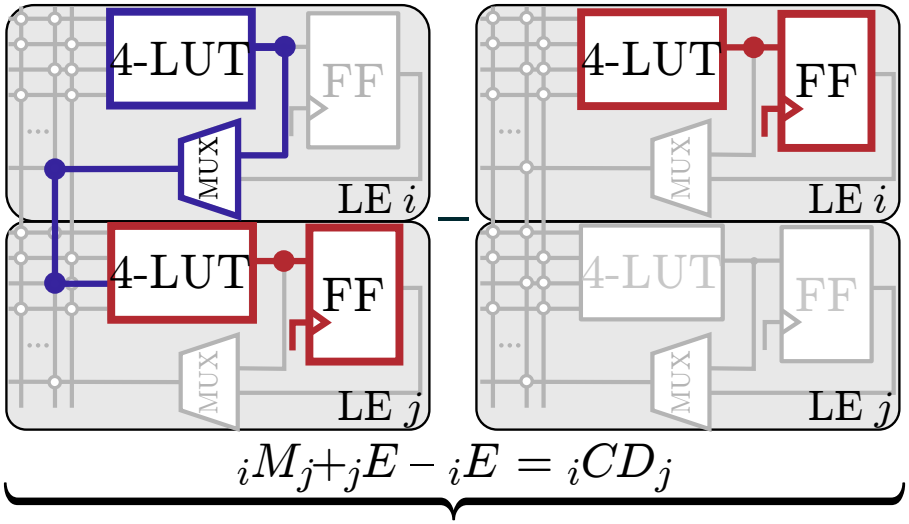
- DUK delays computed from linear combinations of path delays
- Fewer linear combinations $\Rightarrow$ smaller rounding error

Which Paths to Measure?



- DUK delays computed from linear combinations of path delays
- Fewer linear combinations ⇒ smaller rounding error

C-DUKs

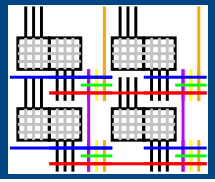


Difference of two paths, both have same prefix.

1. Ends with Nodes ${}_iM_j + {}_jE$
2. Ends with Node ${}_iE$

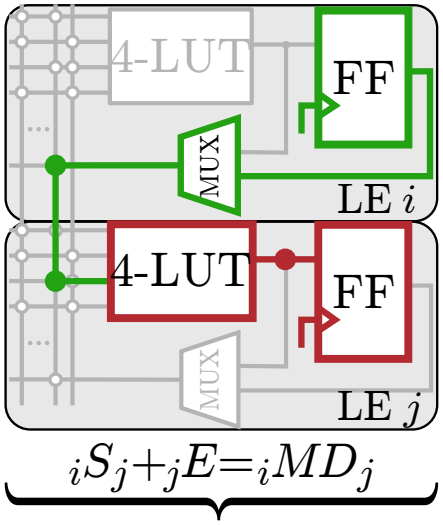
$$(A + {}_iM_j + {}_jE) - (A + {}_iE) = {}_iCD_j$$

Which Paths to Measure?



- DUK delays computed from linear combinations of path delays
- Fewer linear combinations ⇒ smaller rounding error

M-DUKs

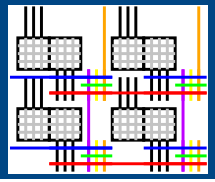


Cannot measure directly (PLL Limit)
Sum of two paths, minus a third.

1. $A + {}_IM_j + {}_jE$
2. ${}_iS_j + {}_jM_k + B$
3. $A + {}_IM_j + {}_jM_k + B$

$$(A + {}_IM_j + {}_jE) + ({}_iS_j + {}_jM_k + B) - (A + {}_IM_j + {}_jM_k + B) = {}_iMD_j$$

Which Paths to Measure?



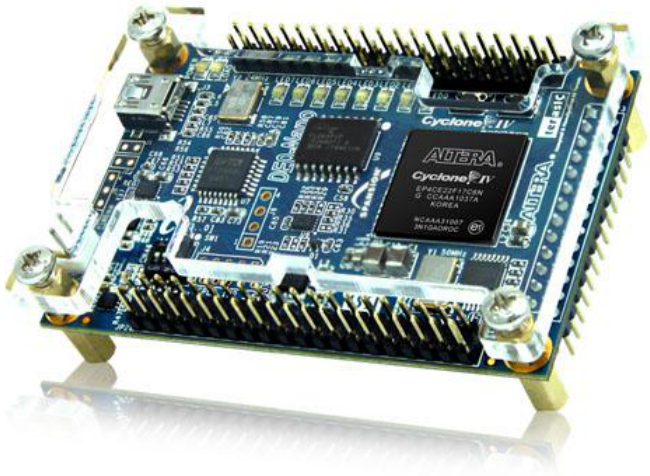
- DUK delays computed from linear combinations of path delays
- Fewer linear combinations $\Rightarrow$ smaller rounding error

- 2 paths per C-DUK
- 3 paths per M-DUK
- Total: $2 \times 480 + 3 \times 480 =$2,400 paths

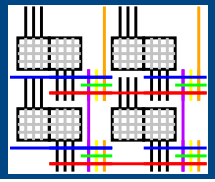
TE on Cyclone III and IV FPGAs

Performed Timing Extraction on LABs

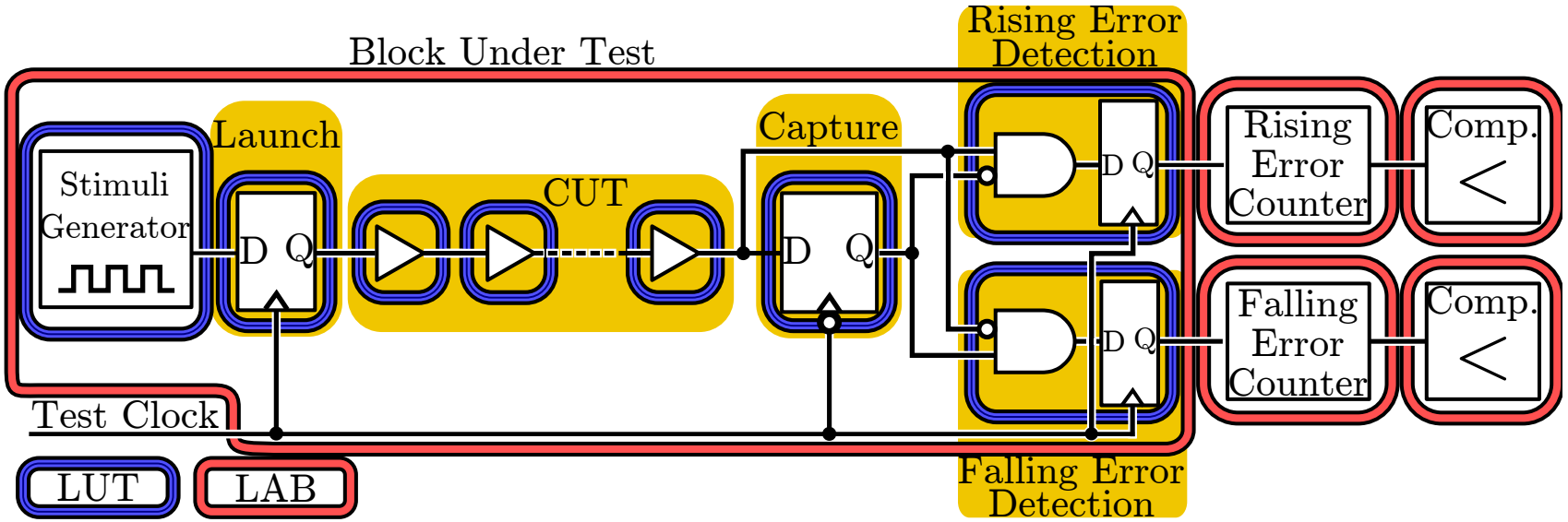
- 18 Altera Cyclone III FPGAs, 65nm
- One Altera Cyclone IV FPGA with V_{dd} control, 60nm
- Measured 2,400 paths per LAB, out of $\approx 10^{18}$



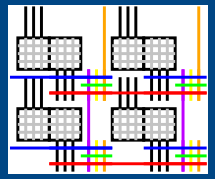
Structured and Systematic Measurements



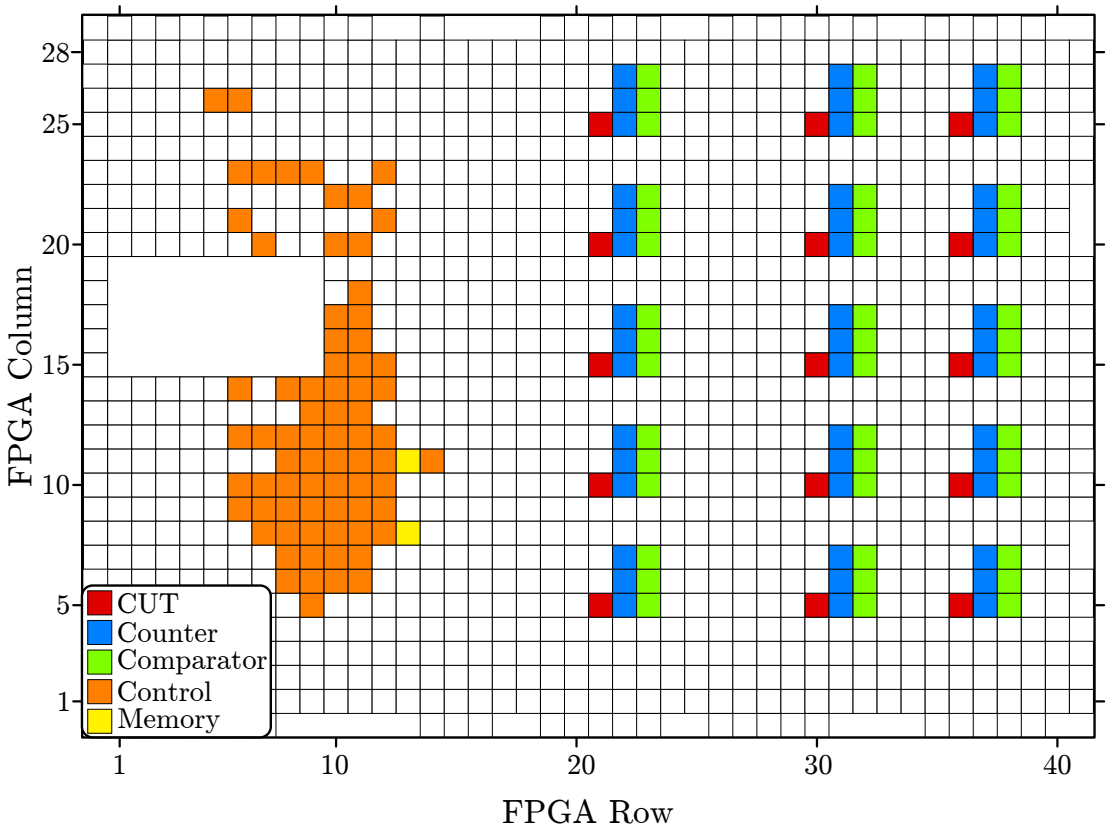
- Controlled placement of Block Under Test



Structured and Systematic Measurements

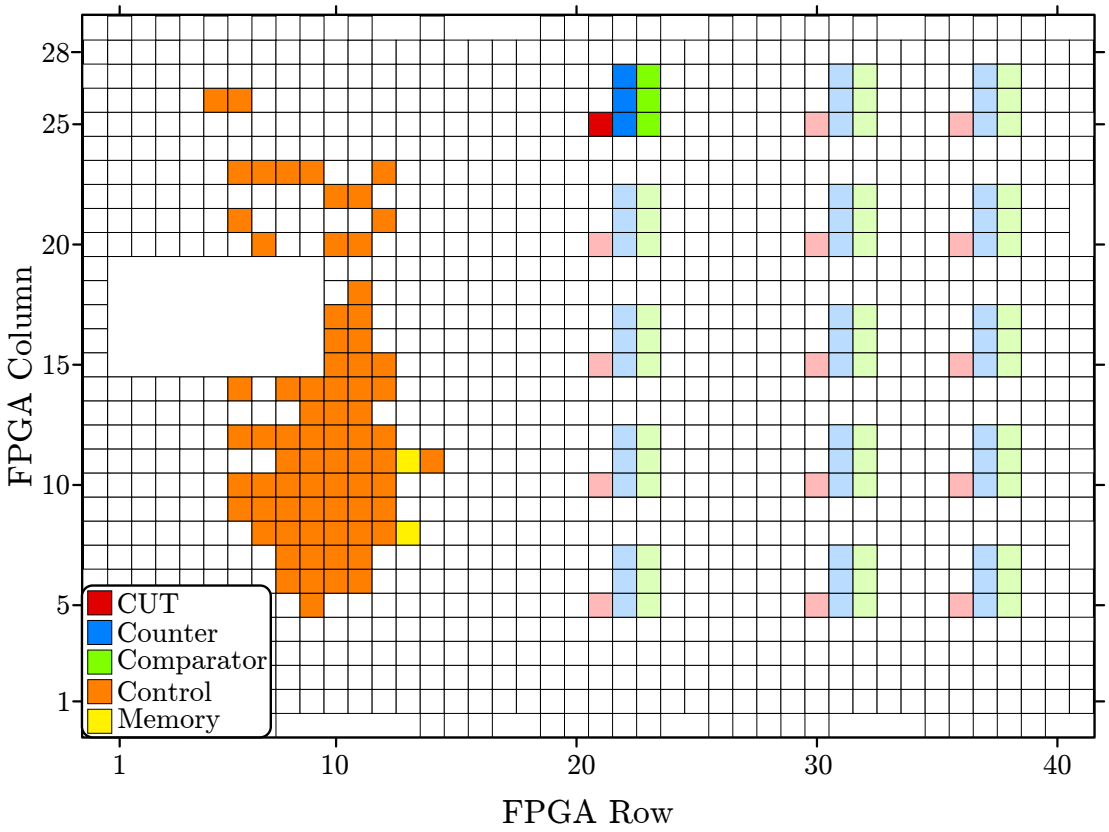


- Controlled placement of Block Under Test
- Isolation of control logic and measurement logic

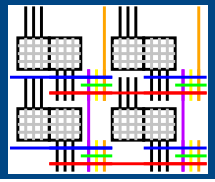


Structured and Systematic Measurements

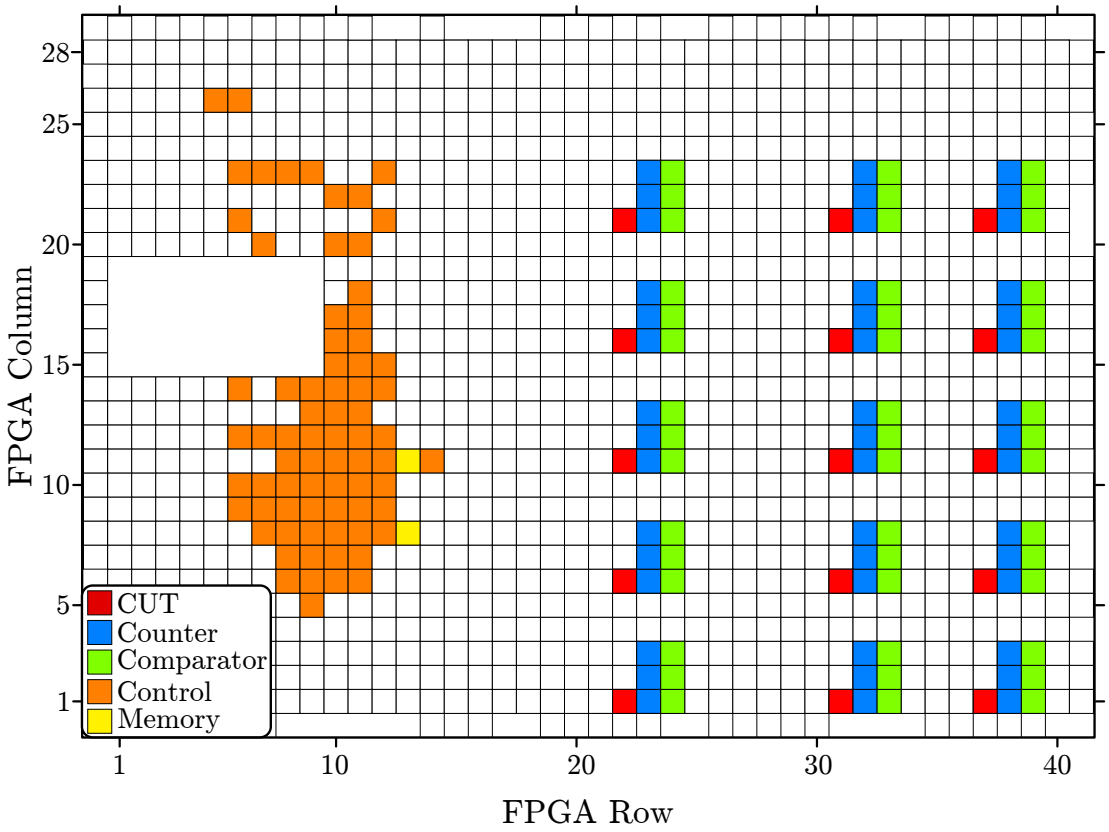
- Controlled placement of Block Under Test
- Isolation of control logic and measurement logic
- Individual LAB Measurements



Structured and Systematic Measurements

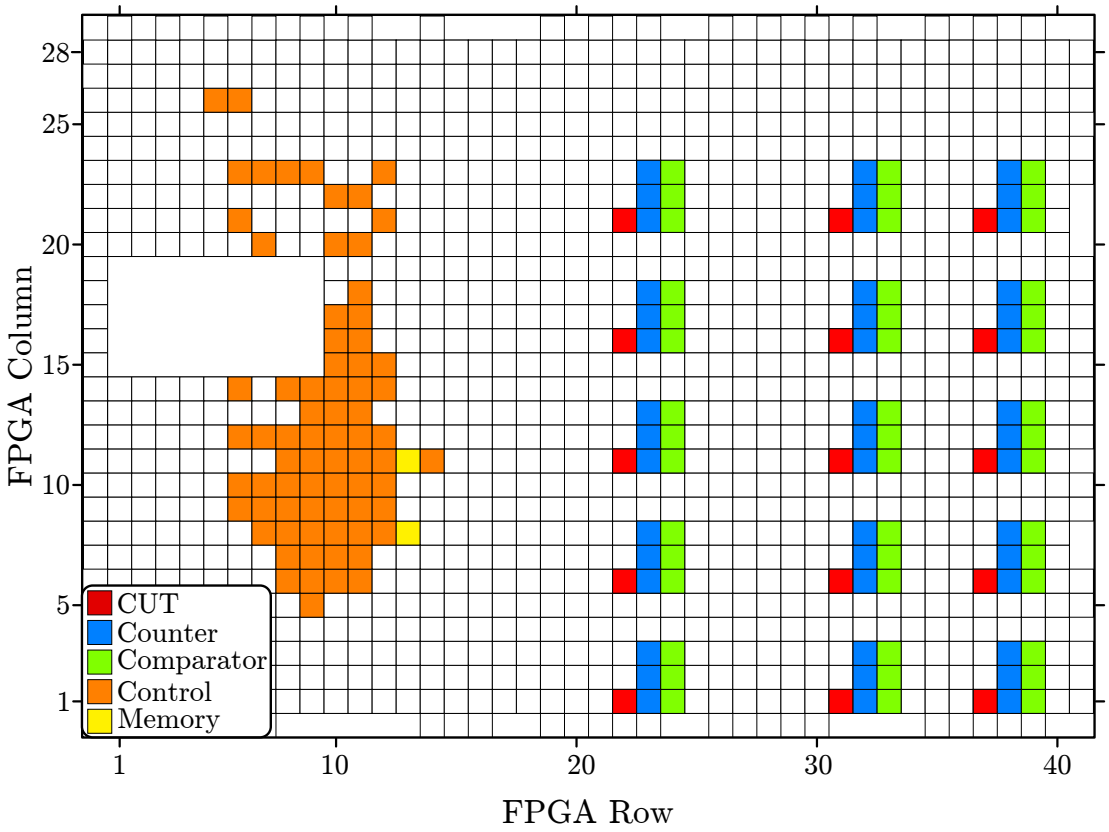


- Controlled placement of Block Under Test
- Isolation of control logic and measurement logic
- Individual LAB Measurements
- Consistent control logic between tests

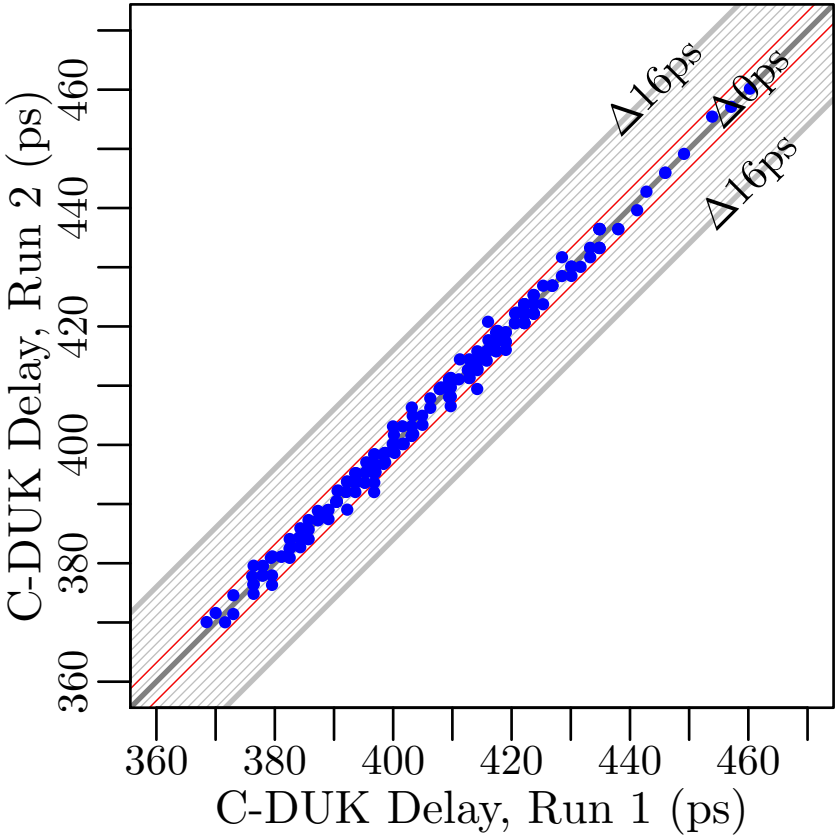


Structured and Systematic Measurements

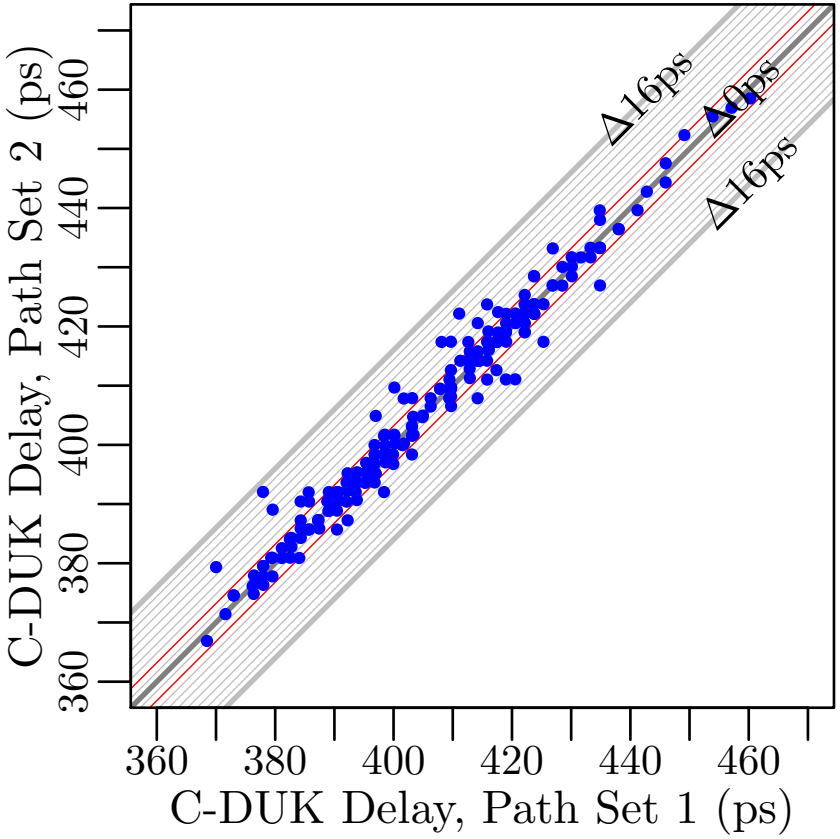
- Controlled placement of Block Under Test
- Isolation of control logic and measurement logic
- Individual LAB Measurements
- Consistent control logic between tests
- Temperature controlled environment



Measurement Confidence



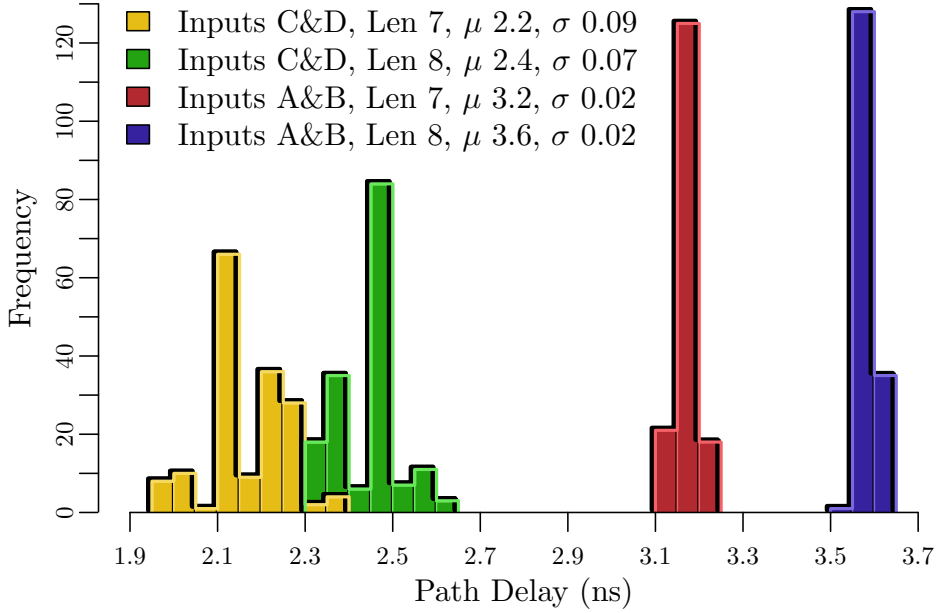
Run vs Run
LAB (27,22)



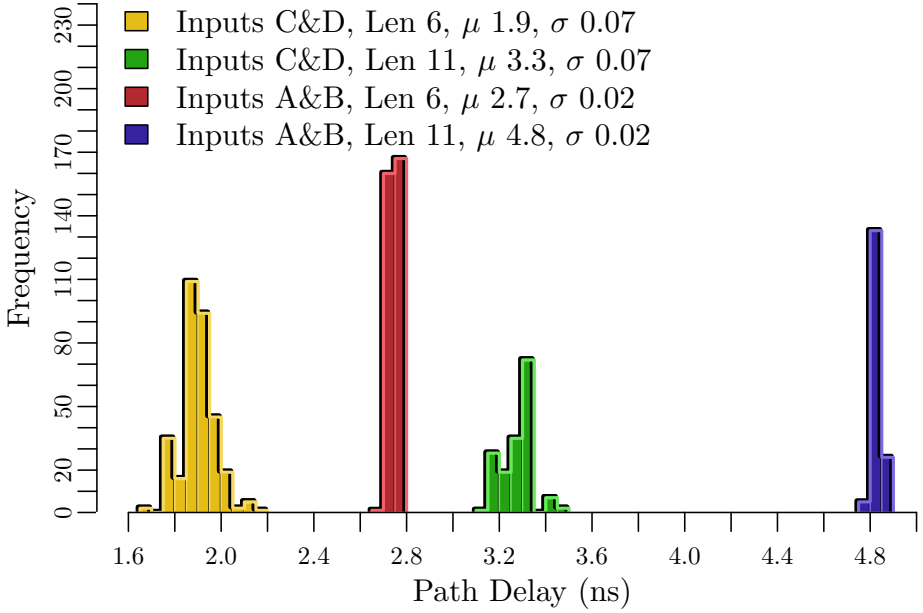
DUK-Equivalent Path Sets
LAB (27,22)

1.6 ps clock granularity

Results: Path Delays

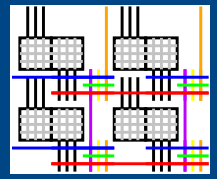


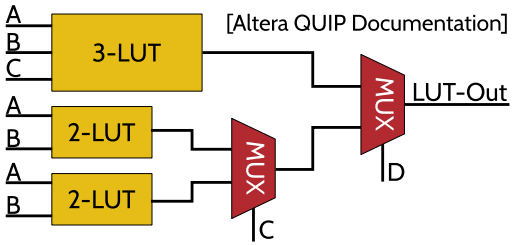
Path delay distribution for C-DUKs. LAB (27,22)

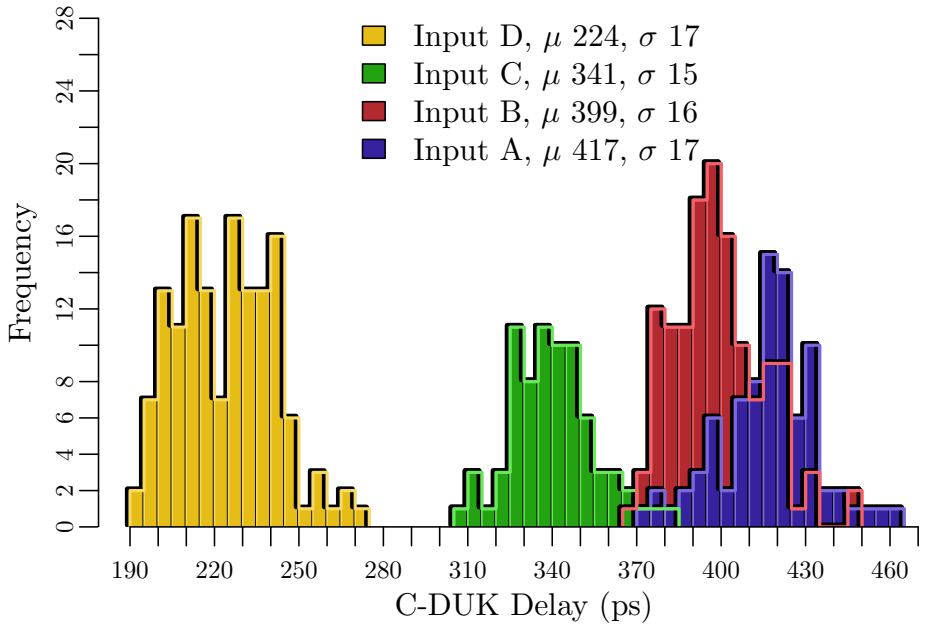


Path delay distribution for M-DUKs. LAB (27,22)

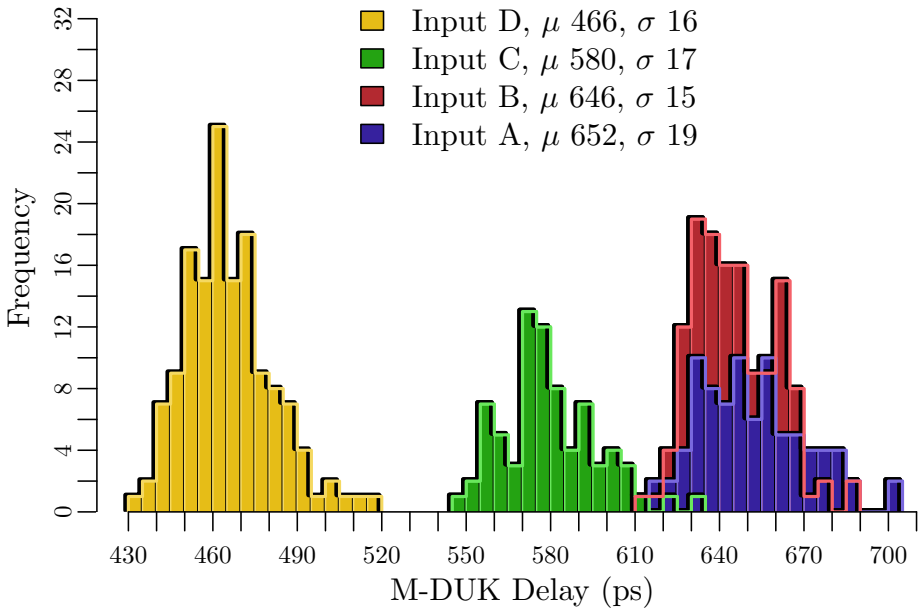
DUK Delays





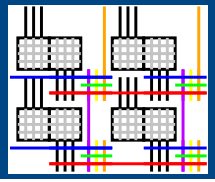


C-DUK delays. LAB (27,22)



M-DUK delays. LAB (27,22)

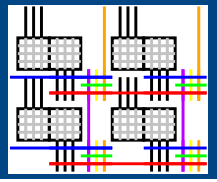
LUT to LUT Delay Map



End LE \ Start LE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		409	384	381	377	389	390	393	393	379	392	395	379	403	382	398
2	400		433	434	403	414	412	420	422	403	417	418	404	422	409	401
3	378	414		409	376	392	395	393	398	382	396	395	379	400	387	376
4	418	417	417		426	434	423	417	420	404	414	431	408	434	409	416
5	385	396	395	419		422	397	401	404	387	399	404	388	407	393	382
6	415	422	423	422	404		453	442	423	406	415	430	411	434	409	415
7	392	388	393	395	373	412		409	390	373	385	398	377	403	377	384
8	396	407	400	401	396	406	409		434	422	409	412	396	417	400	390
9	376	387	387	382	376	387	390	409		392	384	389	370	396	376	368
10	407	419	417	412	411	425	419	423	422		449	445	414	423	409	403
11	379	390	390	385	380	390	393	396	393	414		422	382	396	382	372
12	422	420	422	422	401	418	426	415	417	399	414		426	445	398	409
13	381	388	393	384	379	389	396	398	390	376	396	416		416	377	371
14	417	418	422	412	401	415	428	414	417	398	409	420	399		423	430
15	385	396	401	393	385	398	403	403	403	392	396	401	384	423		398
16	457	460	438	434	414	433	441	430	428	411	425	434	420	438	412	

C-DUK delay (ps)
A & B LUT Inputs
LAB (27,22)

LUT to LUT Delay Map



End LE \ Start LE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		409	384	381	377	389	390	393	393	379	392	395	379	403	382	398
2	400		433	434	403	414	412	420	422	403	417	418	404	422	409	401
3	378	414		409	376	392	395	393	398	382	396	395	379	400	387	376
4	418	417	417		426	434	423	417	420	404	414	431	408	434	409	416
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6	415	422	423	422	404		453	442	423	406	415	430	411	434	409	415
7	392	388	393	395	373	412		409	390	373	385	398	377	403	377	384
8	396	407	400	401	396	406	409		434	422	409	412	396	417	400	390
9	376	387	387	382	376	387	390	409		392	384	389	370	396	376	368
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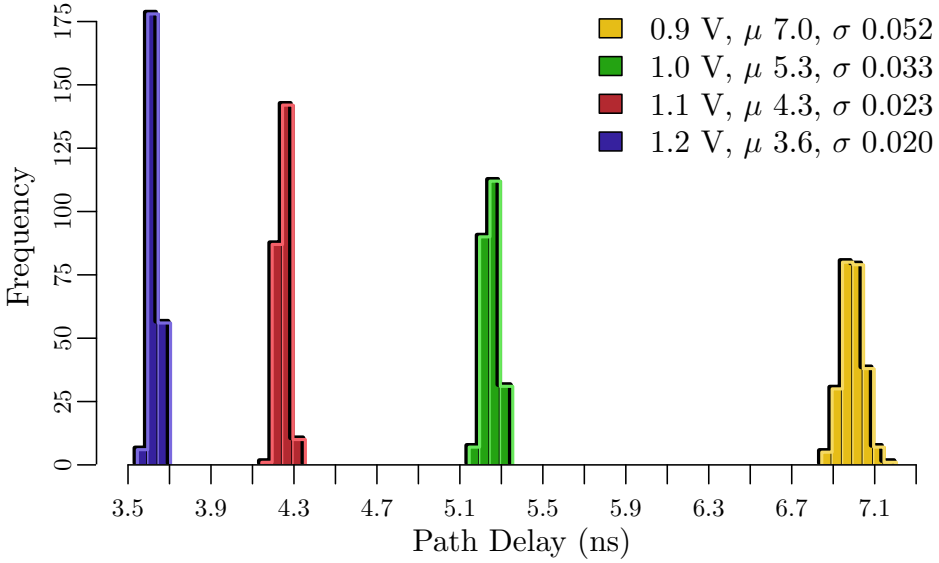
11	379	390	390	385	380	390	393	396	393	414		422	382	396	382	372
12	422	420	422	422	401	418	426	415	417	399	414		426	445	398	409
13	381	388	393	384	379	389	396	398	390	376	396	416		416	377	371
14	417	418	422	412	401	415	428	414	417	398	409	420	399		423	430
15	385	396	401	393	385	398	403	403	403	392	396	401	384	423		398
16	457	460	438	434	414	433	441	430	428	411	425	434	420	438	412	

LAB (27,22)

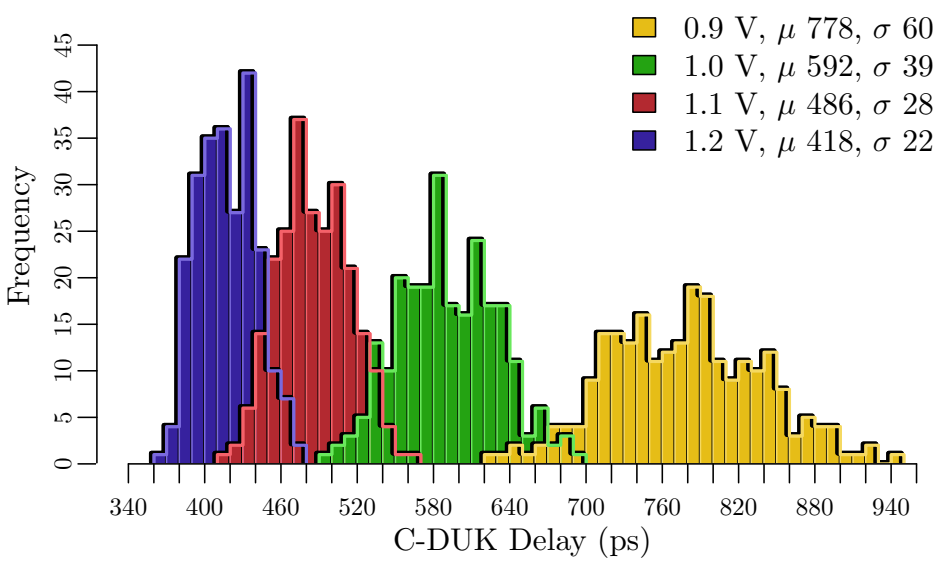
End LE \ Start LE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		415	392	407	376	398	382	385	390	393	384	392	388	401	385	423
2	390		431	450	398	417	396	401	411	418	401	409	407	412	404	418
3	368	407		426	374	396	381	379	390	392	380	387	384	393	379	396
4	401	415	398		422	431	411	398	407	409	399	396	412	415	399	420
5	373	395	388	433		422	382	382	390	396	384	390	387	395	384	396
6	407	430	417	441	417		452	437	417	423	415	411	425	420	409	433
7	392	409	396	422	390	428		411	393	399	391	398	399	409	385	418
8	399	422	415	438	407	426	412		442	447	411	417	412	423	411	423
9	369	395	393	407	376	392	377	398		411	372	380	376	388	372	388
10	400	428	425	434	406	426	407	407	415		437	434	420	420	404	420
11	374	403	396	411	380	398	385	384	387	425		415	391	395	379	393
12	423	439	428	450	425	439	444	422	426	433	428		455	452	415	438
13	371	393	393	406	380	393	382	380	385	388	380	407		412	372	390
14	420	436	422	436	418	431	444	414	420	422	417	409	422		431	453
15	384	404	409	419	392	407	398	392	403	406	385	395	396	423		423
16	442	462	426	444	418	444	444	414	418	426	415	409	428	422	406	

LAB (37,14)

Lowering V_{DD} on Cyclone IV



Path Delay for C-DUKs
LAB (28,22)

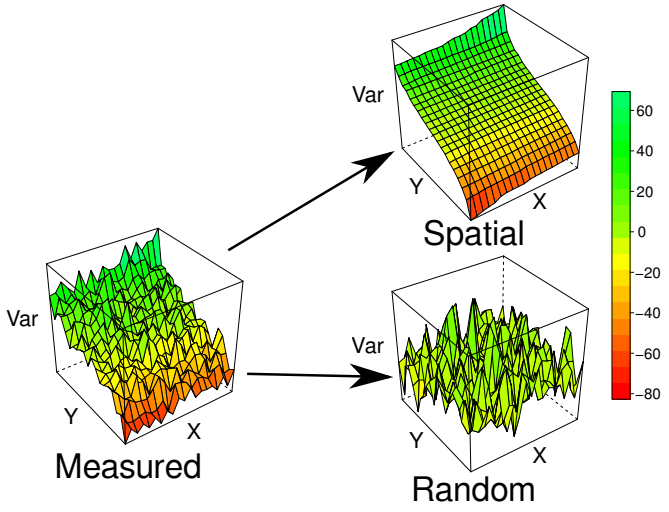


C-DUK Delay
LAB (28,22)

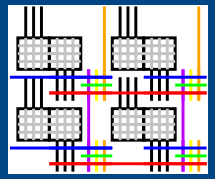
Lower V_{DD} magnifies the impact of random variation

Future Work

- Apply TE to global interconnect
  - Determine necessary DUKs
  - Compute which paths to measure
- Understand necessary level of measurement control
- Comprehensive variation characterization
  - Spatial
  - Systematic
  - Random



Conclusion



Timing Extraction

- Extracts near LUT-level delays
- Uses only resources available in FPGA
- Allows for fine-grain variation characterization
- Generally applicable to modern FPGAs

End LE \ Start LE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		409	384	381	377	389	390	393	393	379	392	395	379	403	382	398
2	400		433	434	403	414	412	420	422	403	417	418	404	422	409	401
3	378	414		409	376	392	395	393	398	382	396	395	379	400	387	376
4	418	417	417		426	434	423	417	420	404	414	431	408	434	409	416
5	385	396	395	419		422	397	401	404	387	399	404	388	407	393	382
6	415	422	423	422	404		453	442	423	406	415	430	411	434	409	415
7	392	388	393	395	373	412		409	390	373	385	398	377	403	377	384
8	396	407	400	401	396	406	409		434	422	409	412	396	417	400	390
9	376	387	387	382	376	387	390	409		392	384	389	370	396	376	368
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12	422	420	422	422	401	418	426	415	417	399	414		426	445	398	409
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14	417	418	422	412	401	415	428	414	417	398	409	420	399		423	430
15	385	396	401	393	385	398	403	403	403	392	396	401	384	423		398
16	457	460	438	434	414	433	441	430	428	411	425	434	420	438	412	