

Memory Block Based Scan-BIST Architecture for Application-Dependent FPGA Testing

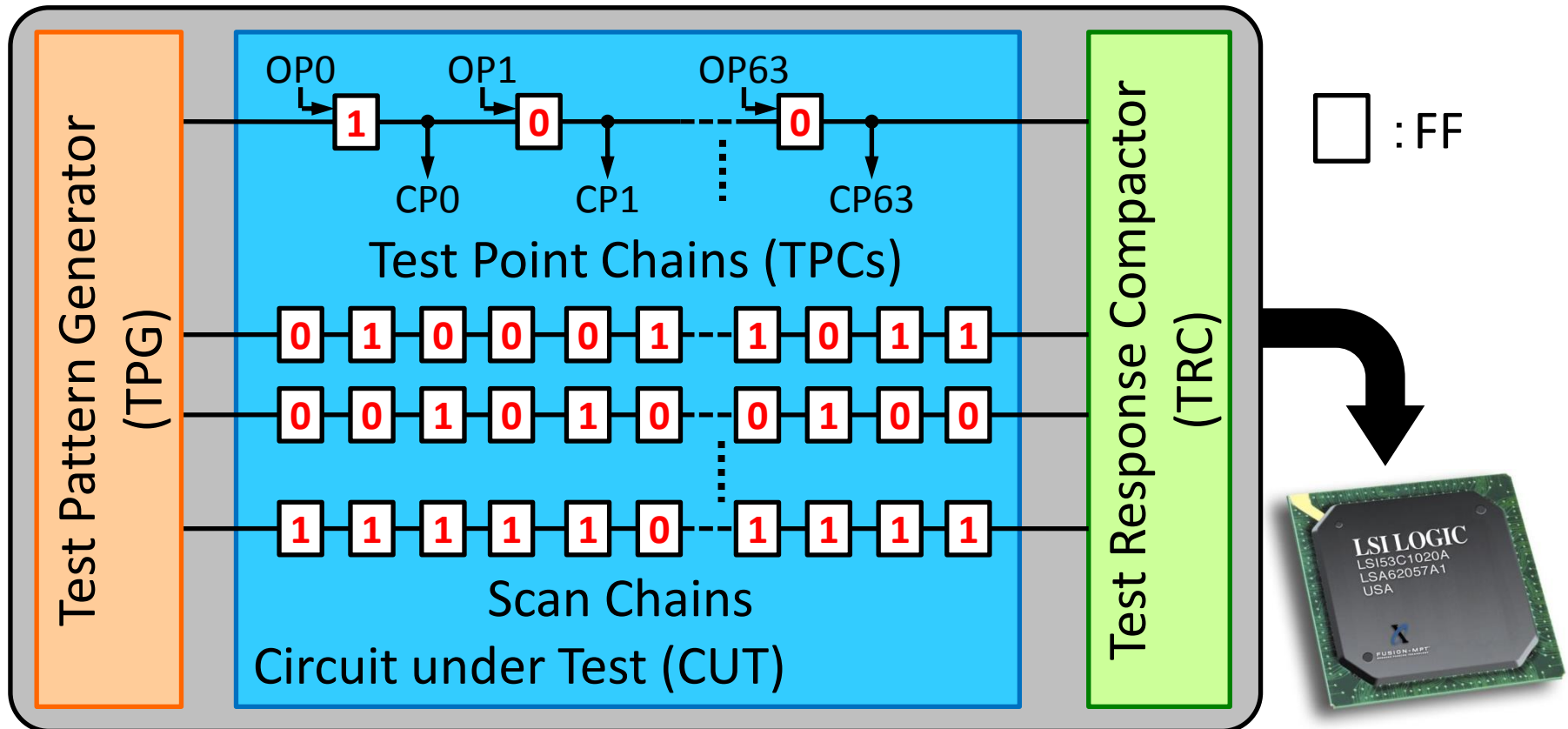
Keita Ito, Tomokazu Yoneda, Yuta Yamato,
Kazumi Hatayama, and Michiko Inoue

Purpose

- Ensure in-field reliability of application circuits on FPGA
 - Concerns: Delay faults due to transistor aging
 - Solution for ASIC: scan-BIST
- BIST: Built-In Self-Test
- Propose FPGA-specific scan-BIST architecture
 - Reduce resource utilization for scan-BIST architecture
 - Improve test quality

Scan-BIST

- Widely used infrastructure for test of ASIC
- Ensure in-field reliability
 - Tester circuits are implemented on a VLSI



Problem and Challenge

- Problems of scan-BIST for FPGA testing
 - Target of conventional BIST is ASIC
 - FPGA is not a scan-ready device

- Many logic elements (LEs) are required to implement scan chains, TPG, TRC and TPCs



Large Logic Elements overhead

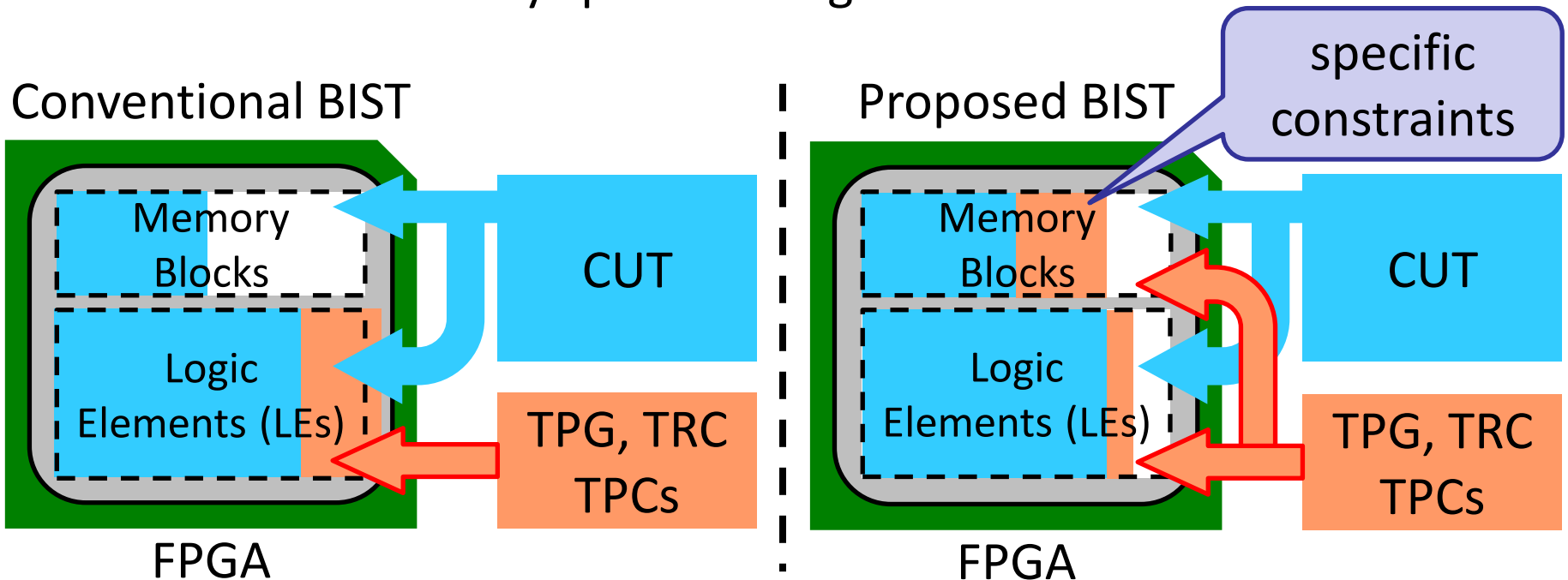
- Challenge
 - FPGA-specific scan-BIST architecture
 - Area-efficient architecture



Reduce Logic Elements usage

Proposed BIST

- Memory Block-based BIST Architecture
 - Use shift register on memory blocks
 - Need to satisfy specific design constraints



Proposed BIST satisfies the constraints

Experimental Results

- Proposed BIST can:
 - reduce the LE usage by using memory blocks
 - achieve higher fault coverage

Design	b17 with scan	Conventional BIST	Proposed BIST	
Resource for Shift Registers	-	LEs	LEs	Memory Blocks
Total LEs	9,334	9,493(+159)	9,911(+577)	9,550(+216)
Total FFs	1,317	1,489	1,997	1,333
Total Memory Bits	0	0	0	424
Fault Coverage	-	49.43 %	54.47 %	

Our Poster

- Conventional Technology
 - Scan-BIST and Test point insertion
- Proposed Method
 - Memory block based scan-BIST architecture
 - Test Application Scheme
- Experimental Results
 - Achieve higher fault coverage
 - Reduce the logic elements usage
- Future Work

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