A Roadmap for Reconfigurable Computing in the DataCenter.

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Workload-Optimized and Hybrid Systems

IBM Research



• AGENDA

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- Current uses of Reconfigurable Logic at IBM
- Limitations
- Capabilities with Power8 / CAPI



- Current and Recent uses of Reconfigurable Logic at IBM
 - Datapower
 - Storage Controller
 - Netezza

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- Texas Memory Systems (Enterprise FLASH)
- Z Enterprise Data Compression

Ideal World?



"LegUp.org" High-Level Synthesis

LegUp accepts a standard C program as input and automatically compiles the program to a hybrid architecture containing an FPGA-based MIPS soft processor and custom hardware accelerators that communicate through a standard bus interface. In the hybrid processor/accelerator architecture, program segments that are unsuitable for hardware implementation can execute in software on the processor.

"Our long-term vision is to fully automate the flow in Fig. 1, thereby creating a self-accelerating adaptive processor in which profiling, hardware synthesis and acceleration happen transparently without user University of Toronto / Altera aware newsy weecg.toronto.edu/~janders/fpga60-legup.pdf



Figure 1: Design flow with LegUp.



Figure 2: Target system architecture.



- Steps in the right direction ...
 - Shared Memory Heterogeneous Architecture
 - No difference in memory model between compute accelerator and CPU core
 - Accelerators are always optional
 - Programming with more Locality Awareness
 - Optimization, not a requirement
 - Usually a good thing to do anyway
 - Programming for predictability
 - Good thing to do anyway
 - Interoperable runtimes and runtime optimization
 - e.g. LLVM
 - Standards-based
 - e.g. OpenCL \rightarrow OpenMP

POWER8



POWER8 Integrated PCIe Gen 3

POWER8



POWER7



Native PCIe Gen 3 Support

- Direct processor integration
- Replaces proprietary GX/Bridge
- Low latency
- Gen3 x16 bandwidth (16 Gb/s)

Transport Layer for CAPI Protocol

- Coherently Attach Devices
 connect to processor via PCIe
 - Protocol encapsulated in PCIe



POWER8 CAPI Coherent Accelerator Processor Interface

Virtual Addressing

- Accelerator can work with same memory addresses that the processors use
- Pointers de-referenced same as the host application
- Removes OS & device driver overhead •

Hardware Managed Cache Coherence
Enables the accelerator to participate in "Locks" as a normal thread Lowers Latency over IO communication model

POWER8





Customizable Hardware

Application Accelerator

- Specific system SW, middleware, or user application
- Written to durable interface provided by PSL ٠

PCle Gen 3

Transport for encapsulated messages

Processor Service Layer (PSL)

- Present robust, durable interfaces to applications
- Offload complexity / content from CAPP •

Advantages of Shared Memory Accelerator

Virtual Addressing

- -Removes the requirement for pinning system memory for PCIe transfers
 - Eliminates the copying of data into and out of the pinned DMA buffers
 - Eliminates the operating system call overhead to pin memory for DMA
- Accelerator can work with same addresses that the processors use
 - · Pointers can be de-referenced same as the host application
 - Example: Enables the ability to traverse data structures
- Elimination of Device Driver
 - Direct communication with Application
 - No requirement to call an OS device driver or Hypervisor function for mainline processing
- Enables Accelerator Features not possible with PCIe
 Enables efficient Hybrid Applications
 - Applications partially implemented in the accelerator and partially on the host CPU
 - -Visibility to full system memory
 - -Simpler programming model for Application Modules



- Where we hope this takes us.
 - More flexible infrastructure
 - E.g. Cloud

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- Innovation pipeline
 - More DataPowers, Netezzas, etc.
- More computer architecture research



Thank You!



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