Analyzing the Impact of Heterogeneous Blocks on FPGA Placement Quality

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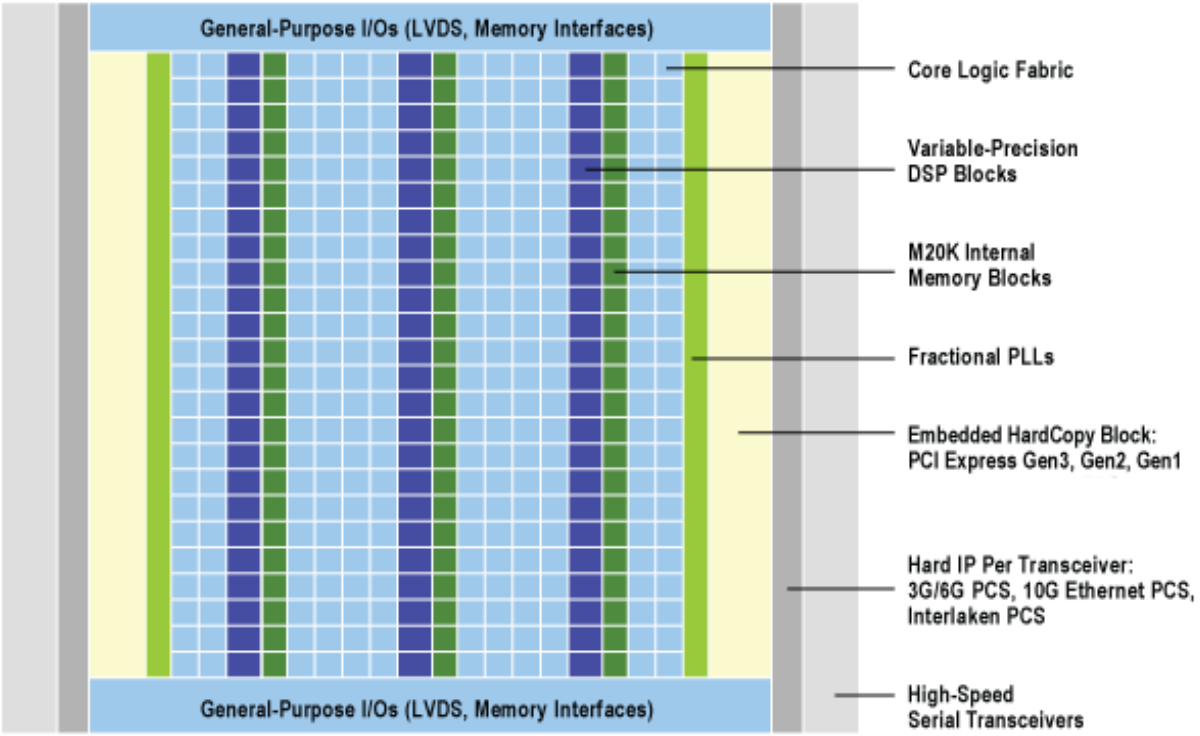
Modern FPGA Device



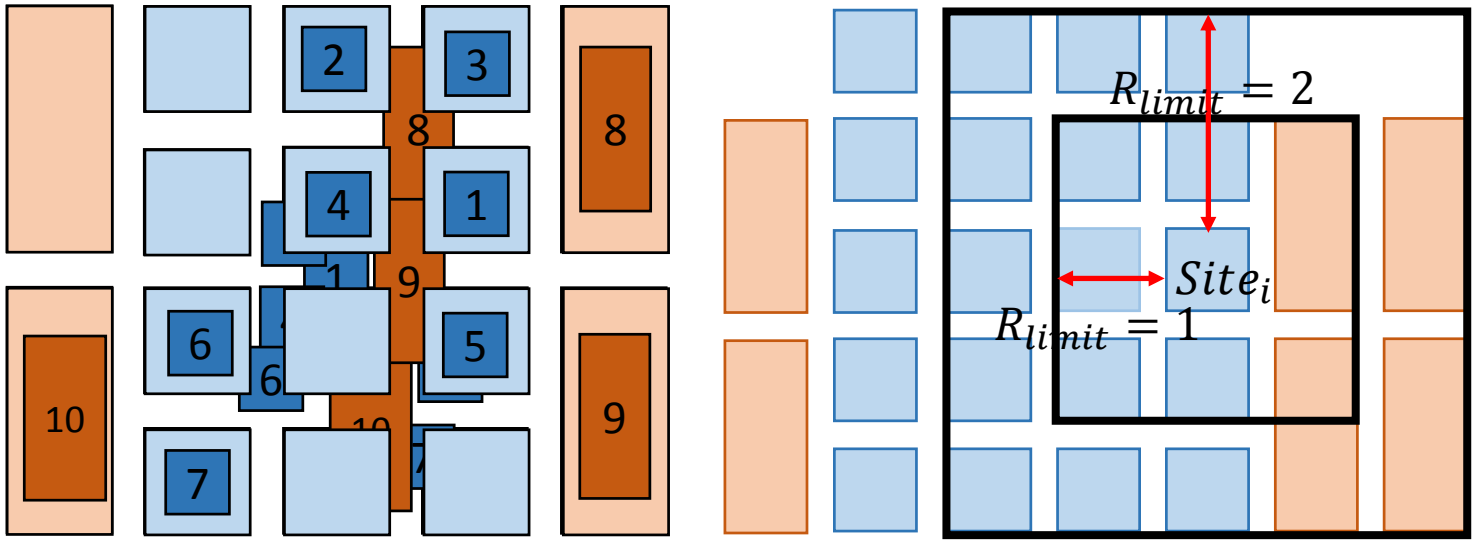
Source: Altera Stratix V FPGA Layout

☞ **Modern FPGAs are heterogeneous.**

e.g., in Stratix V E, there are 359,200 ALMs, 704 DSPs, 2,640 M20Ks, etc.

How do Heterogeneous Blocks Affect FPGA Placement?

- **Pros:** reduce the netlist size (in both #nets and #blocks) by about 30% compared with homogeneous implementation.
- **Cons:** complicate the legalization, and limit the search space.



☞ **We are interested in *quantifying* the impact!**

Previous Quantitative Optimality Study

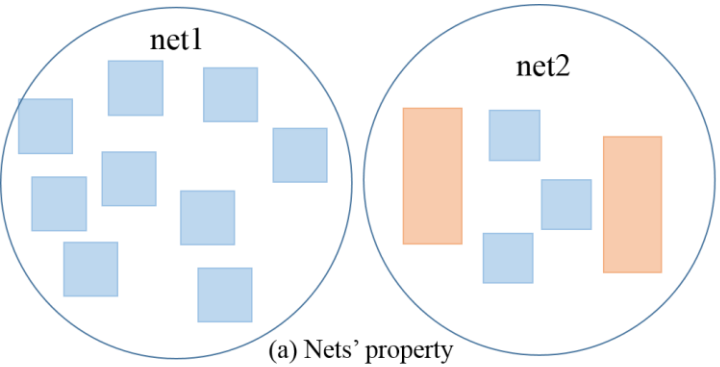
- **PEKO, [Chang et al., TCAD'04]**
  - **Wirelength-optimal benchmarks with blocks of equal size.**
- **PEKO-MS, [Cong et al., Springer'07]**
  - **Examine the optimality of mixed-size ASIC placers.**
- **Constructive, [Papa et al., GLSVLSI'04]**
  - **Examine the constructed patterns visually.**
- **Datapath, [Ward et al., ISPD'11]**
  - **Examine the optimality of datapath placement**

☞ **Ours is the first work to construct wirelength-optimal heterogeneous FPGA placement examples.**

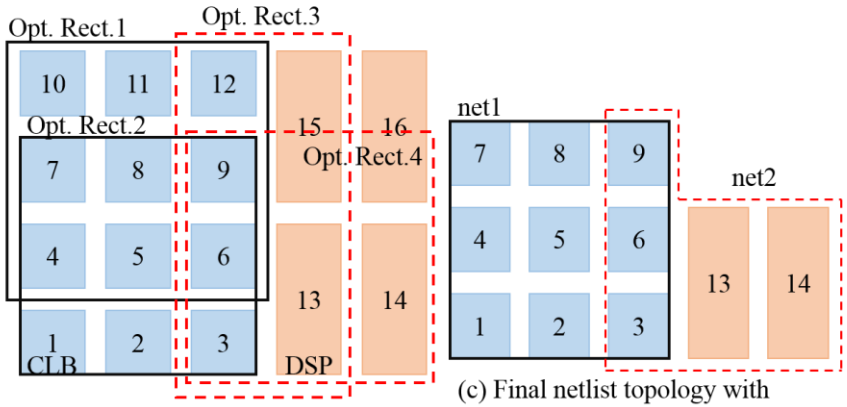
Contributions of This Work

- **Construct synthetic benchmarks with known *optimal half-perimeter wirelength* for heterogeneous FPGAs.**
- **Evaluate the optimality gap of two popular FPGA placers: *VPR* and *Quartus*.**
- **Separately analyze the optimality gap from two sources: *architectural heterogeneity* and *netlist heterogeneity*.**

Synthetic Benchmark Generation: Basic Idea



(a) Nets' property



(b) Heterogeneous Arch.

(c) Final netlist topology with optimal HPWL of 8

1. Given the reference netlist property & heterogeneous arch.

2. Construct optimal net implementation among its **optimal rectangles**, which are obtained by **one-dimensional search**.

3. The netlist with optimal HPWL is generated by implementing each net one by one.

Synthetic Benchmark Generation

- **Optimal rectangle:** a rectangle with minimum half perimeter that can accommodate all types of blocks in a net.
- **One-dimensional search:**
  - For example, a net with 3 "blue" and 2 "organge" blocks
- **Repeated patterns of arch.**
  - Reduce search space.

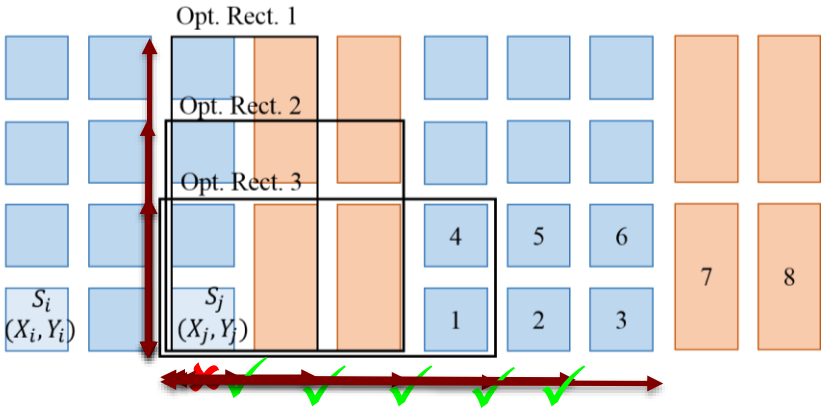


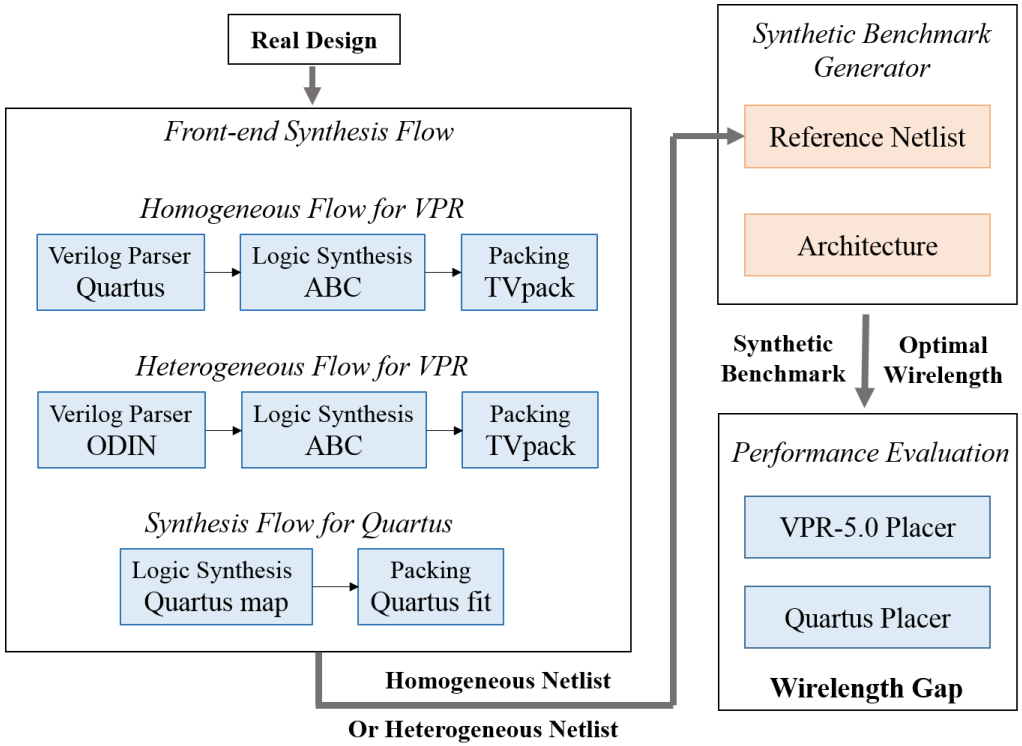
TABLE I
RECTANGLES ACHIEVED IN THE SEARCH PROCESS BY TAKING $S_i(S_j)$ AS AS STARTING POINT

S_i					
l_x	1∼3	4	5	6	7
l_y	∞	4	2	2	2
l_x+l_y	∞	8	7	8	9

S_j		Rect. 1	Rect. 2	Rect. 3		
l_x	1	2	3	4	5	6
l_y	∞	4	3	2	2	2
l_x+l_y	∞	6	6	6	7	8

☞ **The optimal rectangles can be explored offline and reused for the same architecture.**

Quantify the Placement Quality: Evaluation Flow



- **Flow-A:** homogeneous netlist with known opt. HPWL on homogeneous arch.
- **Flow-B:** homogeneous netlist with known opt. HPWL on heterogeneous arch.
- **Flow-C:** heterogeneous netlist with known opt. HPWL on heterogeneous arch.

Quantify the Placement Quality: Optimality Gap

- **Wirelength Gap (WG):**

$$WG = \frac{WL_{placed} - WL_{optimal}}{WL_{optimal}}$$

- **WG for VPR and Quartus placer**
  - **Flow-A on VPR: avg. WG = 33%**
  - **Flow-B on VPR: avg. WG = 40%**
  - **Flow-C on VPR: avg. WG = 48%**
  - **Flow-C on Quartus: avg. WG = 116%**

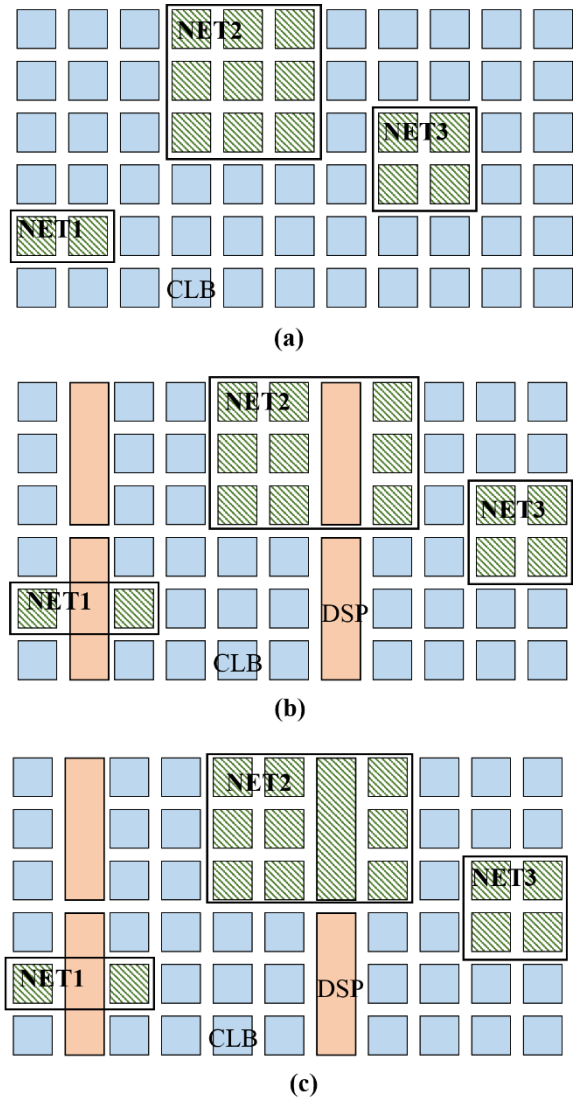
☞ **Netlist topologies are different with different flows!**

Sources of Optimality Gap

- The optimality gap comes from two sources
  - Architectural heterogeneity
    - Solution space becomes much more discrete
  - Netlist heterogeneity
    - Easier to be trapped in a local optimum

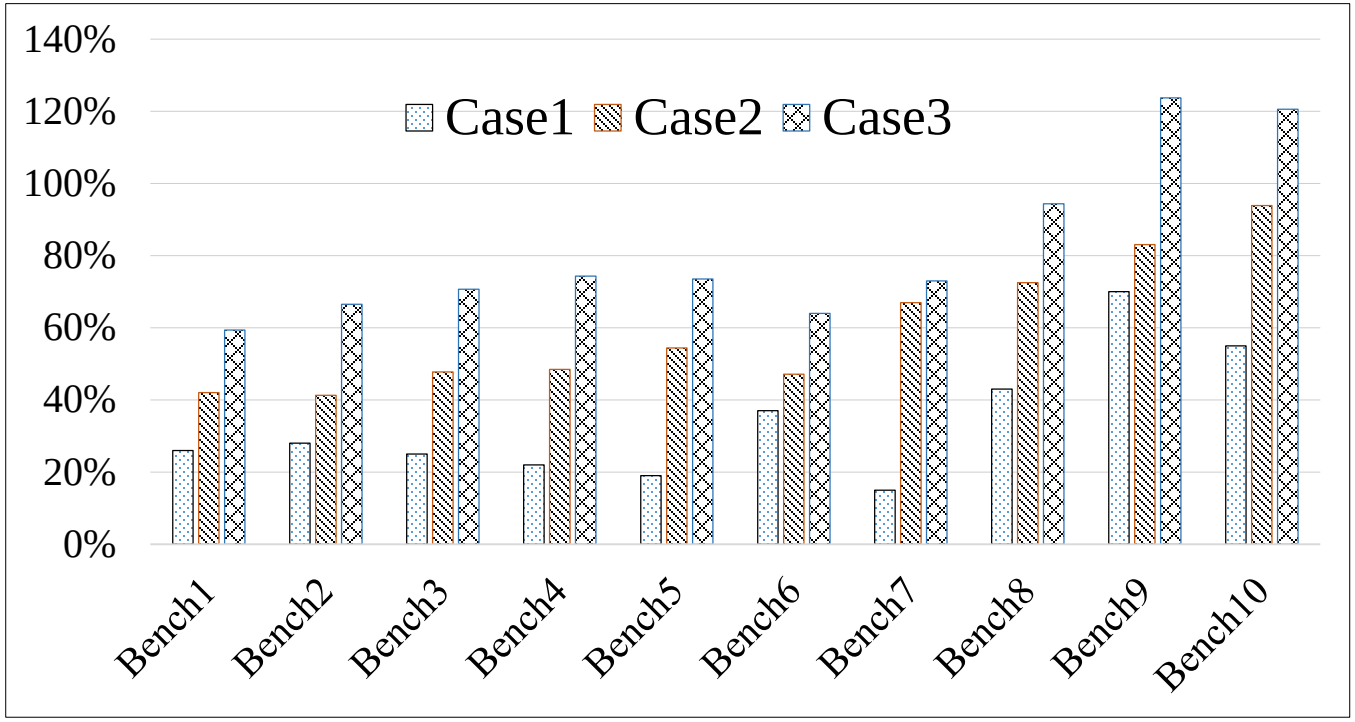
☞ We will quantify the impacts from these two source.

Impacts from the Two Sources: Experiment Design



- **Case-1:** the same as Flow-A.
- **Case-2:** based on Case-1, expanding homogeneous arch. into heterogeneous arch. by adding heterogeneous tiles.
- **Case-3:** based on Case-2, adding H-blocks to homogeneous netlist to generate heterogeneous netlist.
  - On average 5.2% are H-blocks

Impacts from the Two Sources: Experimental Results



- **Base: 33% WG**
- **Architectural heterogeneity: an extra 25% WG**
- **Netlist heterogeneity: an extra 27% WG**

Conclusions

- **An algorithm to construct benchmarks with known optimal wirelength for heterogeneous FPGA placement.**
- **Benchmarking results of VPR placer shows:**
  - **For netlists with the same "functionality"**
    - **Optimality gap for homogeneous design is 33% on average**
    - **Optimality gap for heterogeneous design is 48% on average**
    - **Benefit of netlist size reduction is canceled out by heterogeneity**
  - **For netlists with the same size**
    - **Base optimality gap: 33%**
    - **Architectural heterogeneity: an extra 25%**
    - **Netlist heterogeneity: an extra 27%**

Thank you!

Synthetic Benchmarks Download

https://github.com/FPGAStudy/placement

(in VPR format and Altera VQM format)