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FCUDA:
Friendly Front-ends for FPGA Fast-Start

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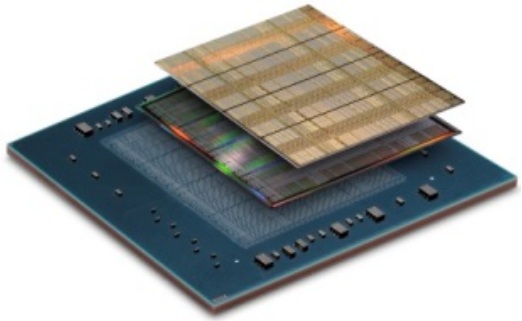
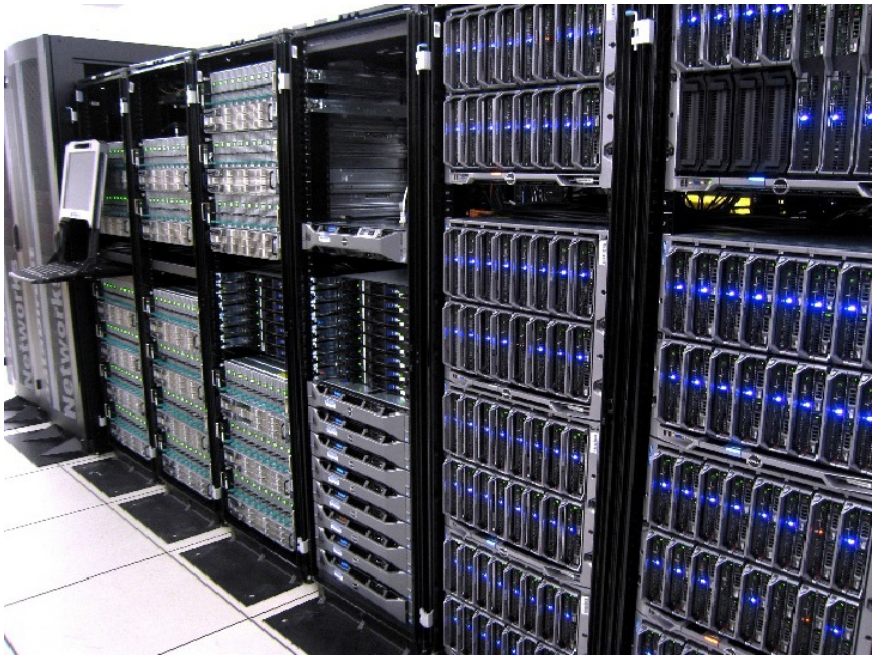
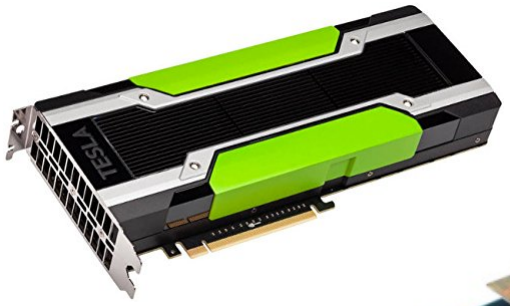
What is Fast-Start

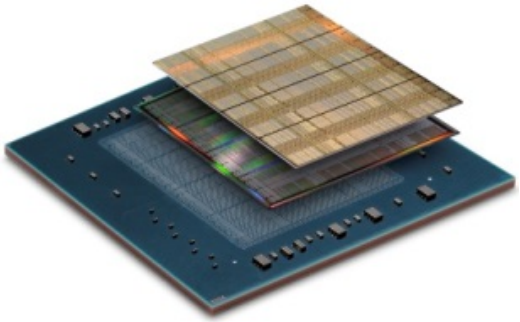


- Low startup to initial solution
- Familiar programming interface
- Fast development iteration
- Development flow
  - Kernel
  - Debugging
  - System-level design
  - Platform integration

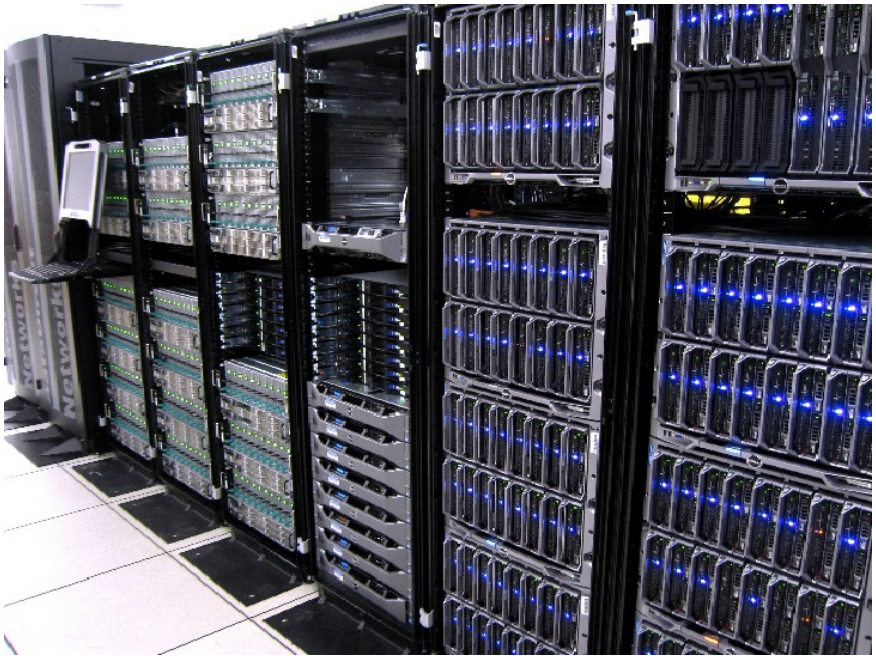


Motivations



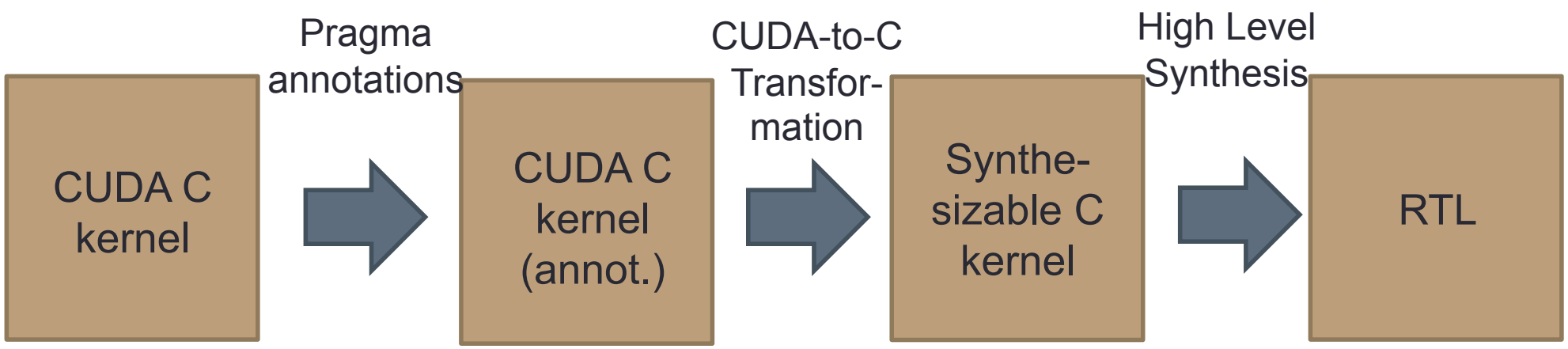


- GPUs and FPGAs: accelerators in HPC
  - NVIDIA GPUs (Google, Baidu, Blue Waters supercomputer,
  - FPGAs (Microsoft Bing search, …)
- NVIDIA GPUs
  - Massively parallelism thanks to the CUDA programming model
  - Power hungry
- FPGAs
  - Low energy consumption, high flexibility
  - Low programming abstraction
  - → High Level Synthesis
  - But parallelism extraction may be limited



FCUDA

- FCUDA Introduction
  - CUDA-to-RTL compiler (ASAP'09, FCCM'11, DAC'13)
  - Front-end: CUDA-to-C (Cetus + MCUDA)
  - Back-end: C-to-RTL (High Level Synthesis tool --Vivado HLS)
- Source-to-source transformation
- Does not employ NVIDIA compiler infrastructure (NVCC, NVMM IR, ...)



FCUDA History

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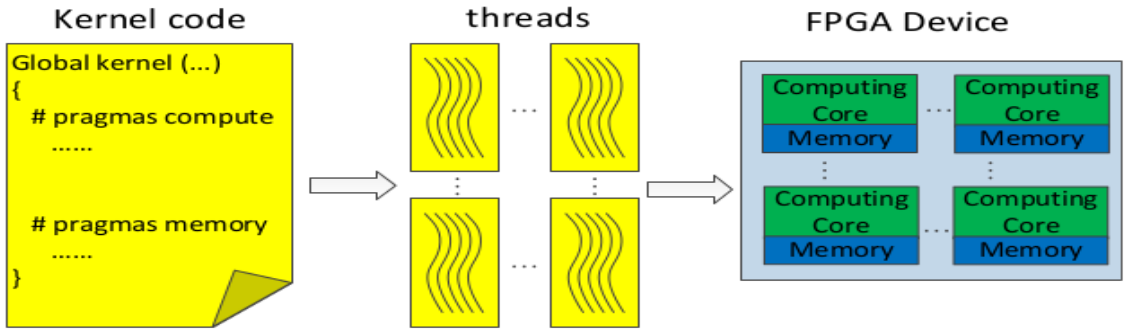
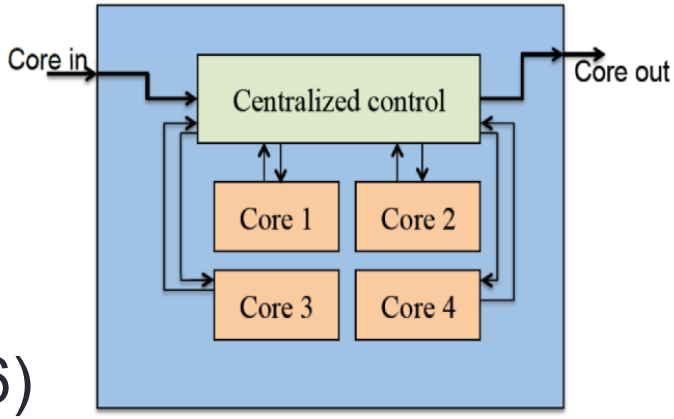
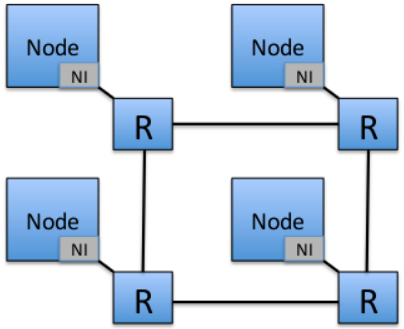
- Does not employ NVIDIA compiler infrastructure (nvcc, nvvm, ...)
- Why FCUDA?
  - Enable CUDA kernel's execution on FPGA
  - CUDA's SIMD programming model is attractive to FPGA



FCUDA System Backend

- Prior FCUDA works focused on building a “prototype”
  - Single top-level function with centralized control of cores
  - No discussion on a full system integration of cores vs. external memory
- System implementation works:
  - FCUDA NoC: Mesh-based NoC (TVLSI’15)
  - FCUDA HB: Hierarchical AXI Bus (TCAD’16)
  - FCUDA SoC: (FPGA’16)





FCUDA Open-source

- Available to download at: http://dchen.ece.illinois.edu/tools.html
- The open-source software includes:
  - FCUDA CUDA-to-C compiler
  - FCUDA Benchmarks: set of benchmarks for testing FCUDA
  - FCUDA SoC tool flow: scripts for the automation of FCUDA system on SoC platform
- In the next few weeks:
  - FCUDA NoC, FCUDA HB, Design Space Exploration framework