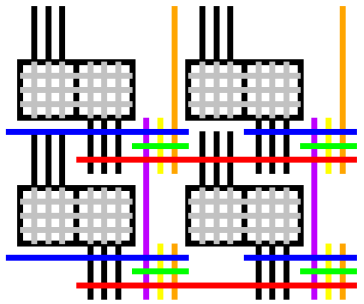

Energy Minimization in the Time-Space Continuum

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Penn

Energy Minimization

- Time-Multiplexed FPGAs save energy?
  - Trimberger [FCCM 1997] says no
  - DeHon [FPGA 2013] says theoretically
- Key issues
  - FPGAs long wires consume most energy
  - TM reduce area, reduce wire lengths
    - But add energy for memories and wire sharing
- Can TM FPGAs reduce wires enough
  - To provide net win versus added costs
- Show TM does **not** reduce energy

Outline

- Review Spatial, Time-Multiplexed
  - How we turn the knob space→time
- Time-Multiplexed Optimization
- Sweep space (time-space continuum)
- Why come out the way it did?
- Sensitivity
- Conclude

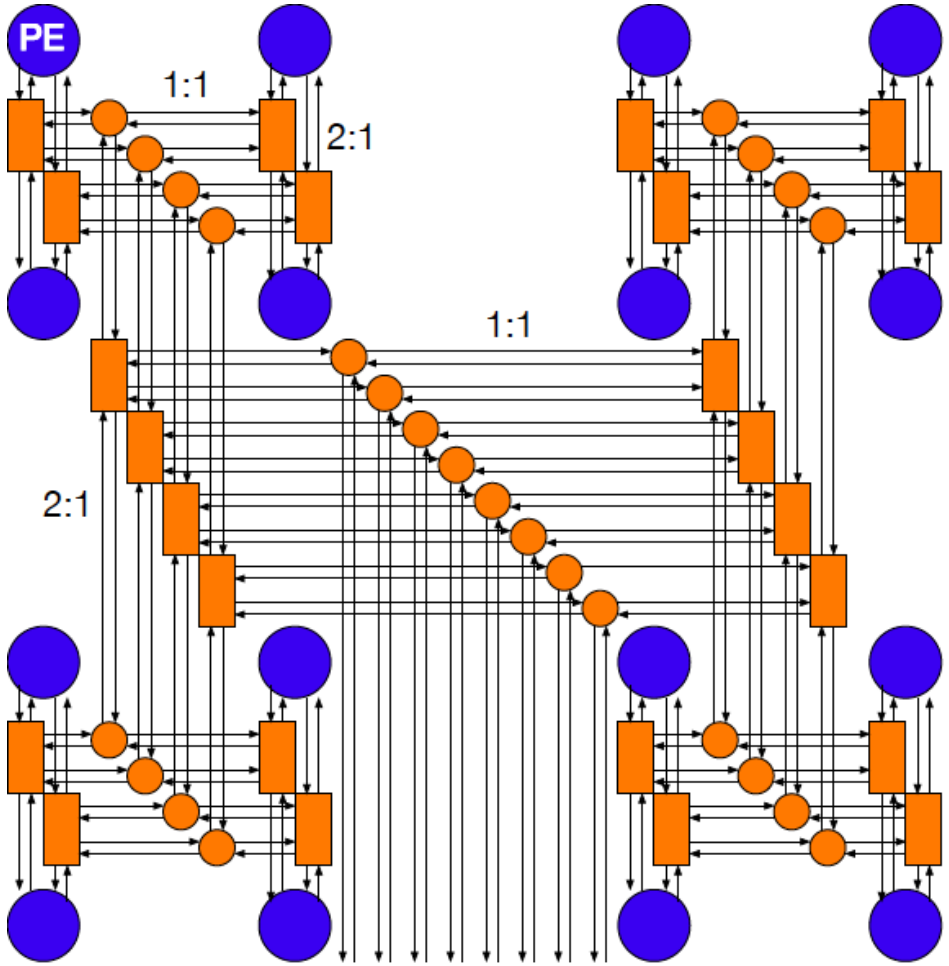
Circuit Level Energy

$$E \propto \alpha C V^2$$

- C driven by wire lengths
  - Including wire lengths and uses in memory
- Elaborate designs to circuit and wire level
- Estimate areas and wire lengths
  - See papers for details

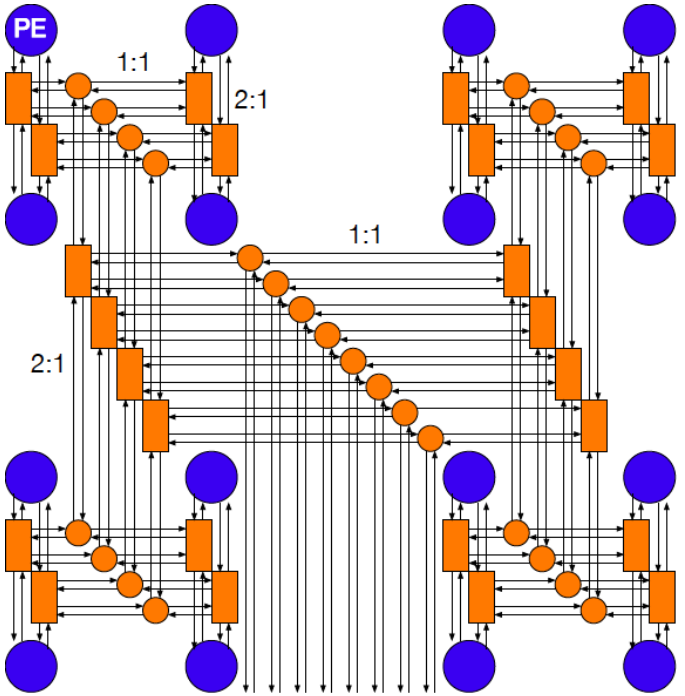
Spatial Design

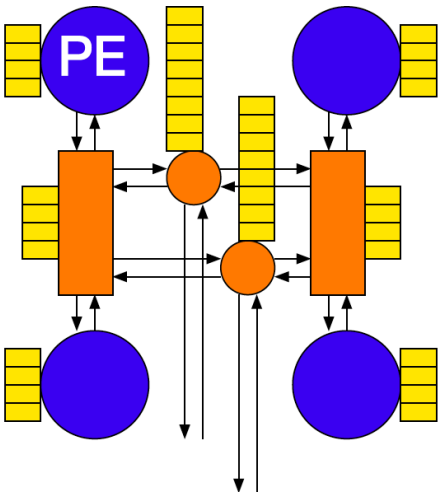
- PE per LUT
- Network connect LUTs
  - Dedicate wire per net
- Allow Locality
  - Short connections
- Place exploit locality
  - Minimize long nets
  - Minimize channel widths
- Tune Rent Parameters



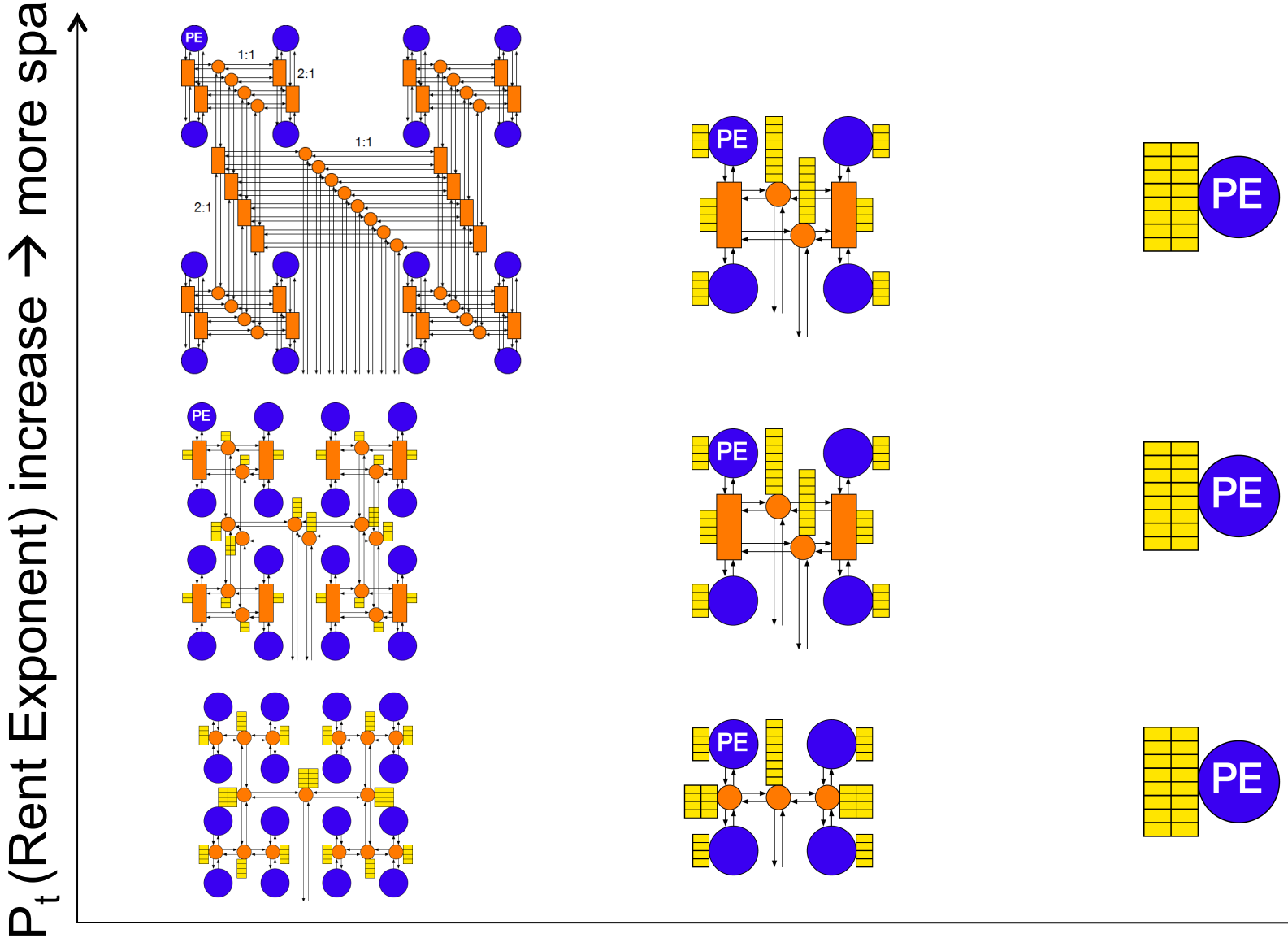
Time Multiplexed Design

- Sequence multiple LUTS on each PE
  - 4 LUTs/PE shown
- Sequence nets on wires, switches
  - Fewer wires
- Add memories
  - Data, Instructions
- Exploit same locality
- Tune Rent Parameters

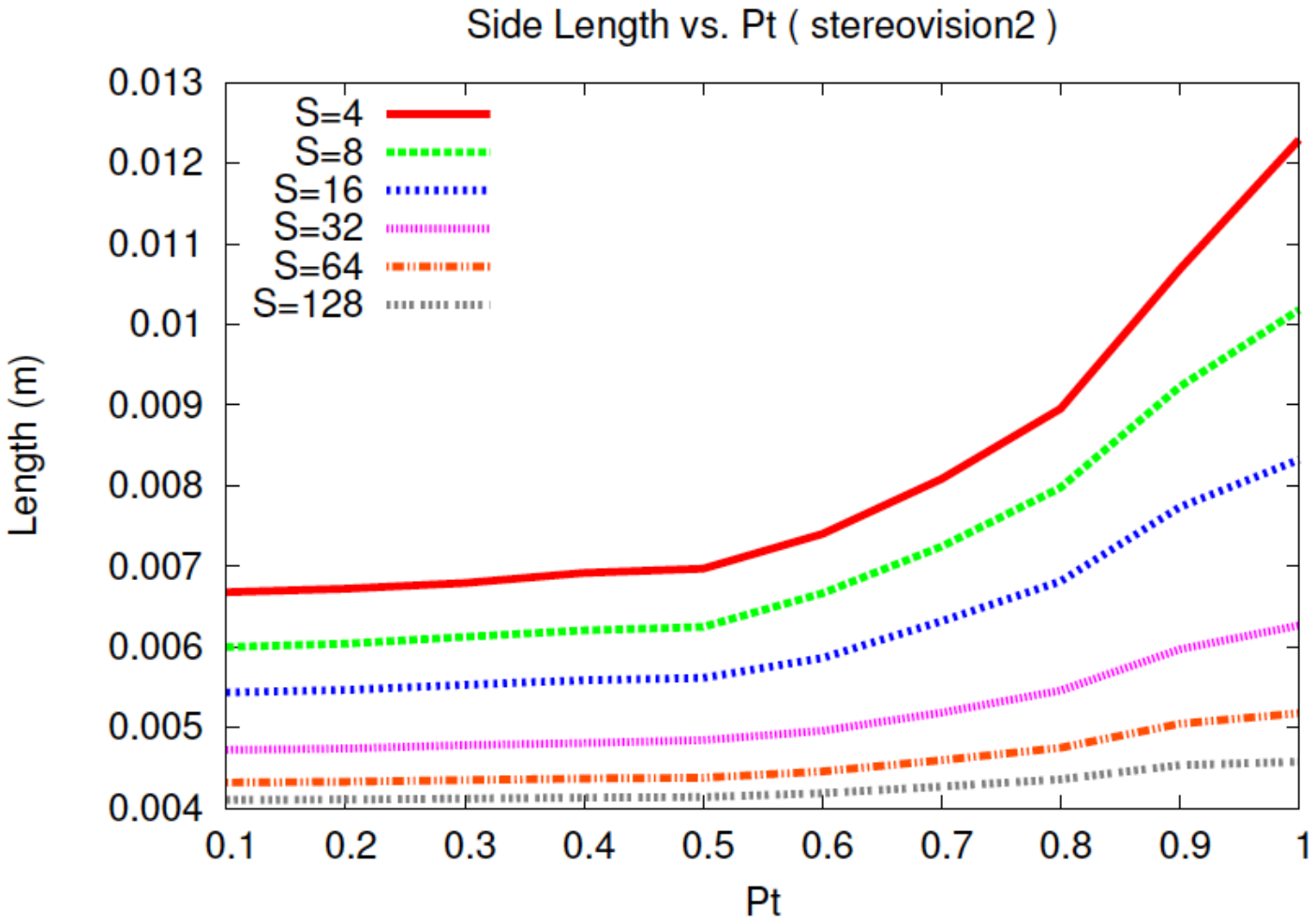




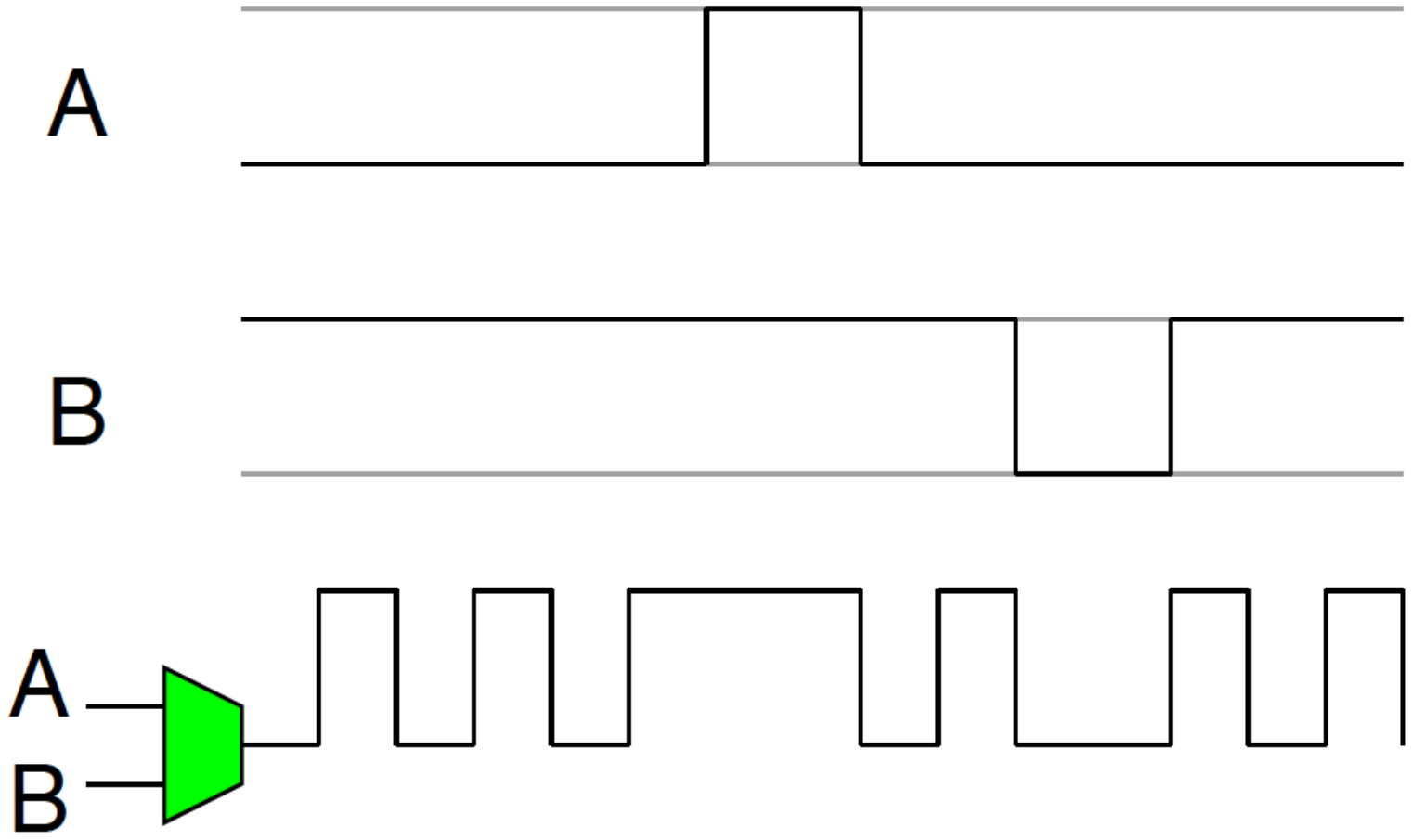
Space-Time Continuum



Time Multiplexing Reduces Wirelength



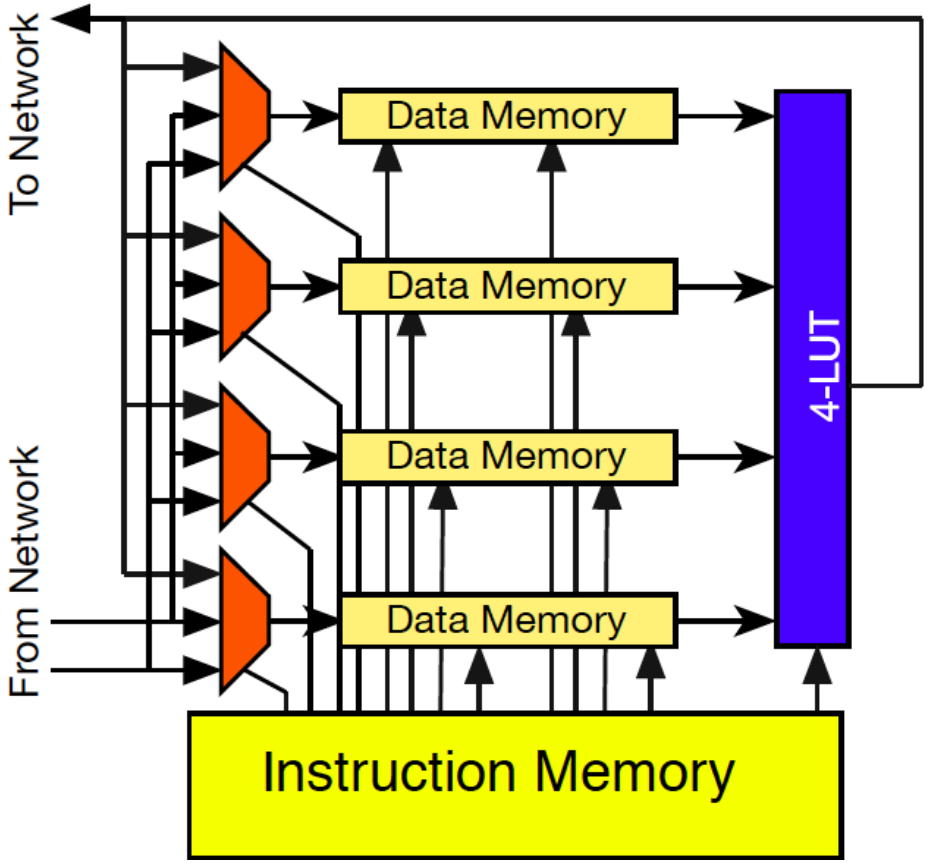
Time Multiplexing Decorrelates Signals → ↑α



Spatial 2 transitions + 2 transitions → 12 transitions

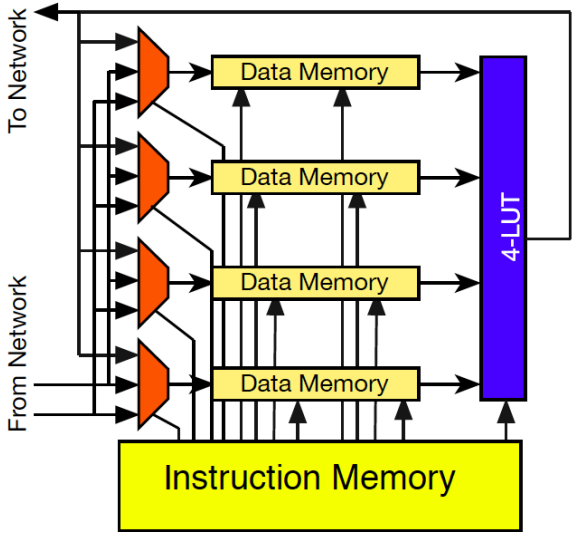
Time Multiplexing Adds Memories

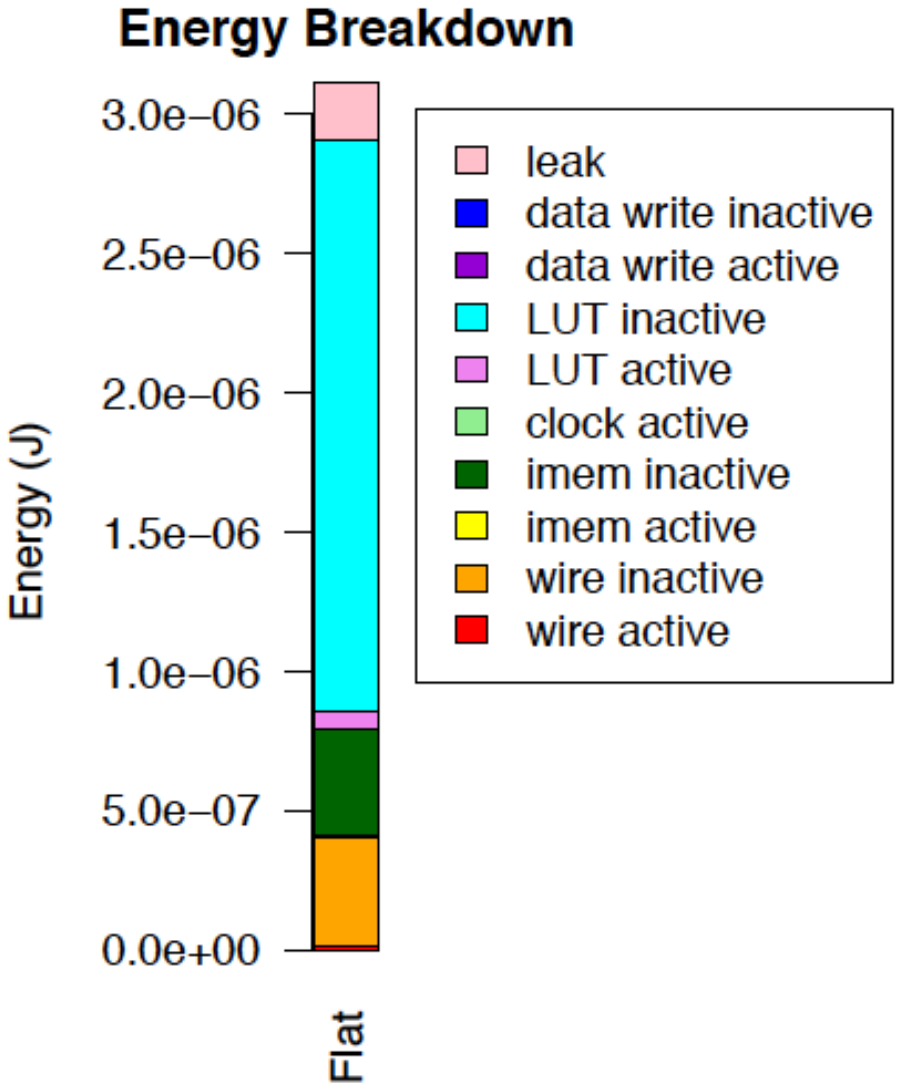
- Memories
  - Data
  - Instructions
- Costs energy to read from memories (and write data)



TM Memory Can Dominate

- Flat Design
- Memory dominates





Outline

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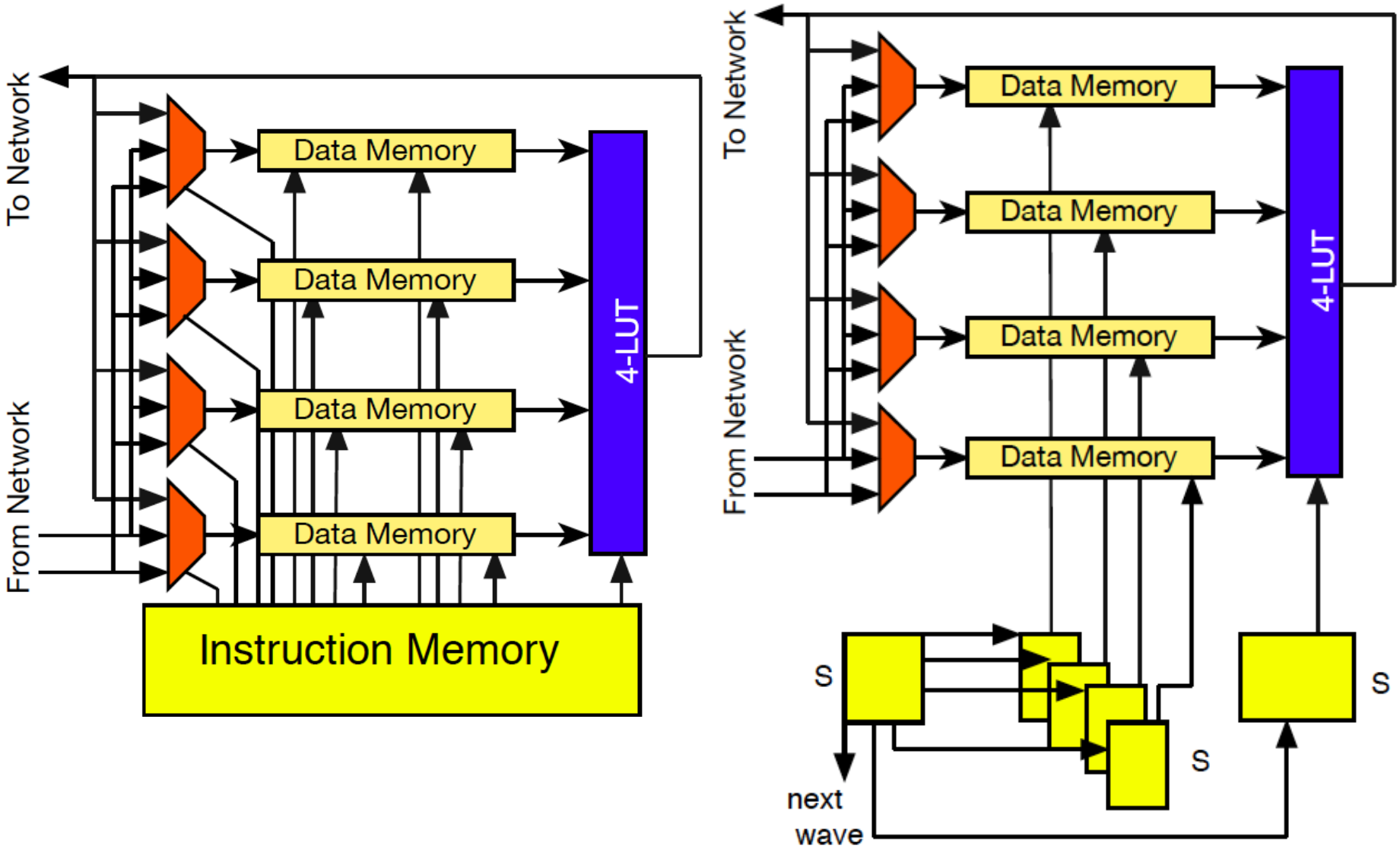
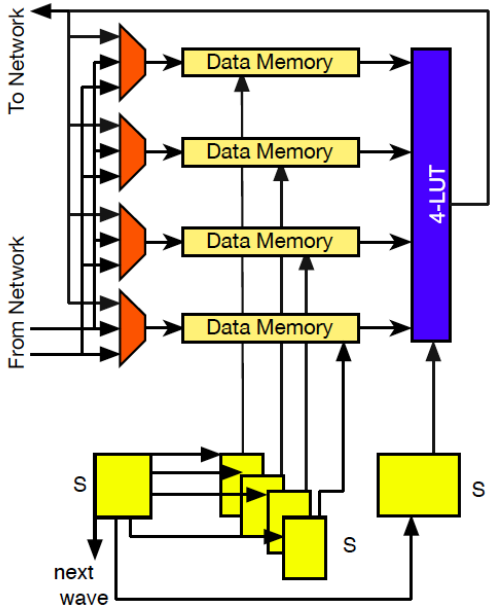
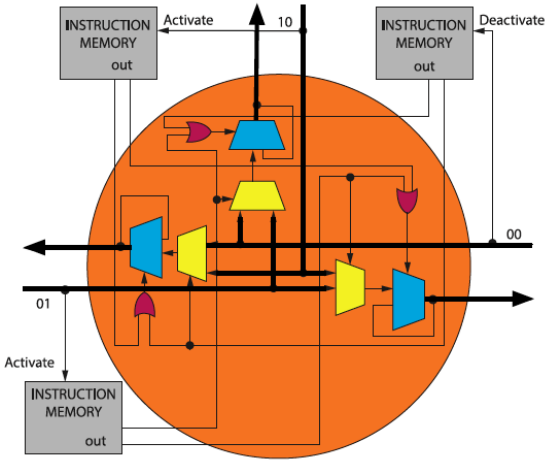
- Sweep space
- Why did it come out the way it did?
- Sensitivity
- Conclude

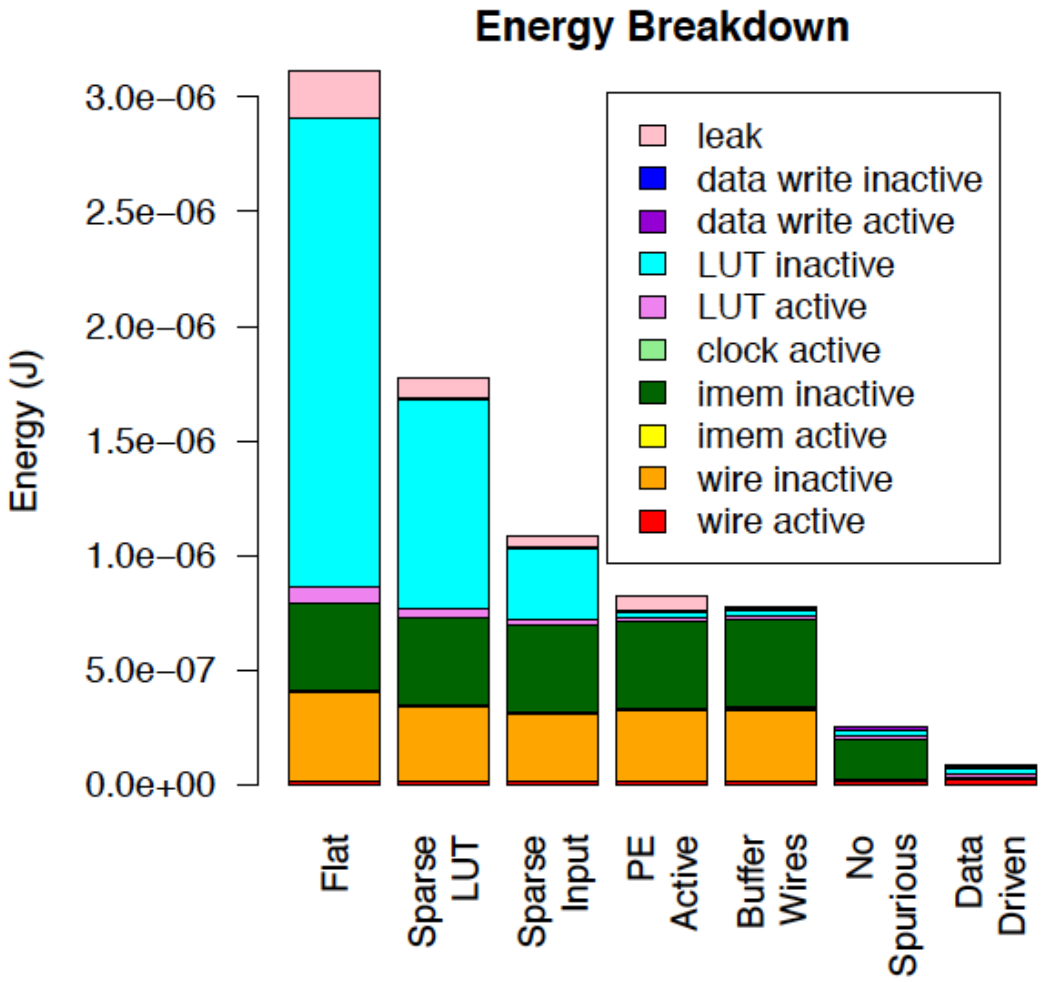
TM Fully Sparse



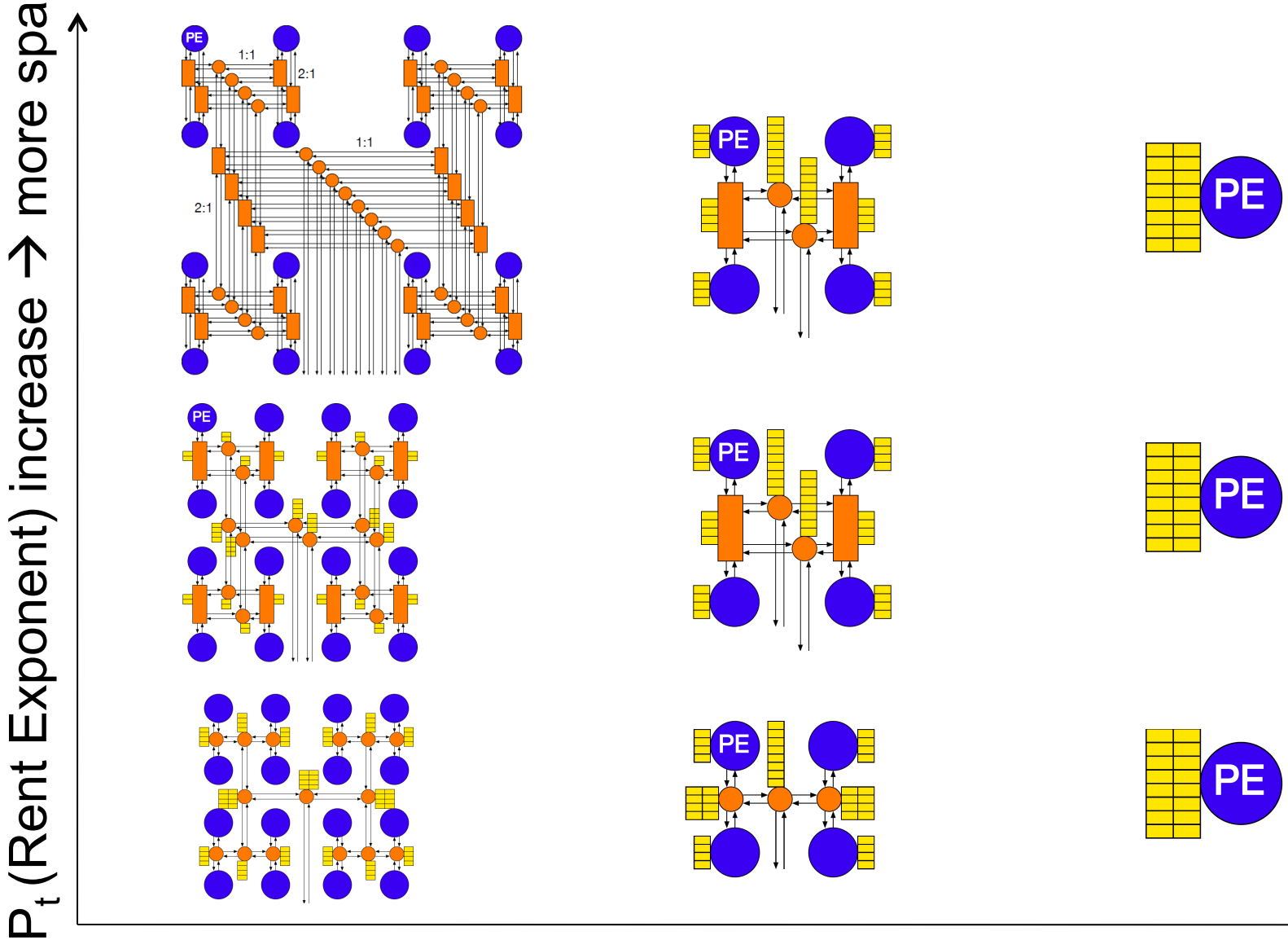
TM Data Driven



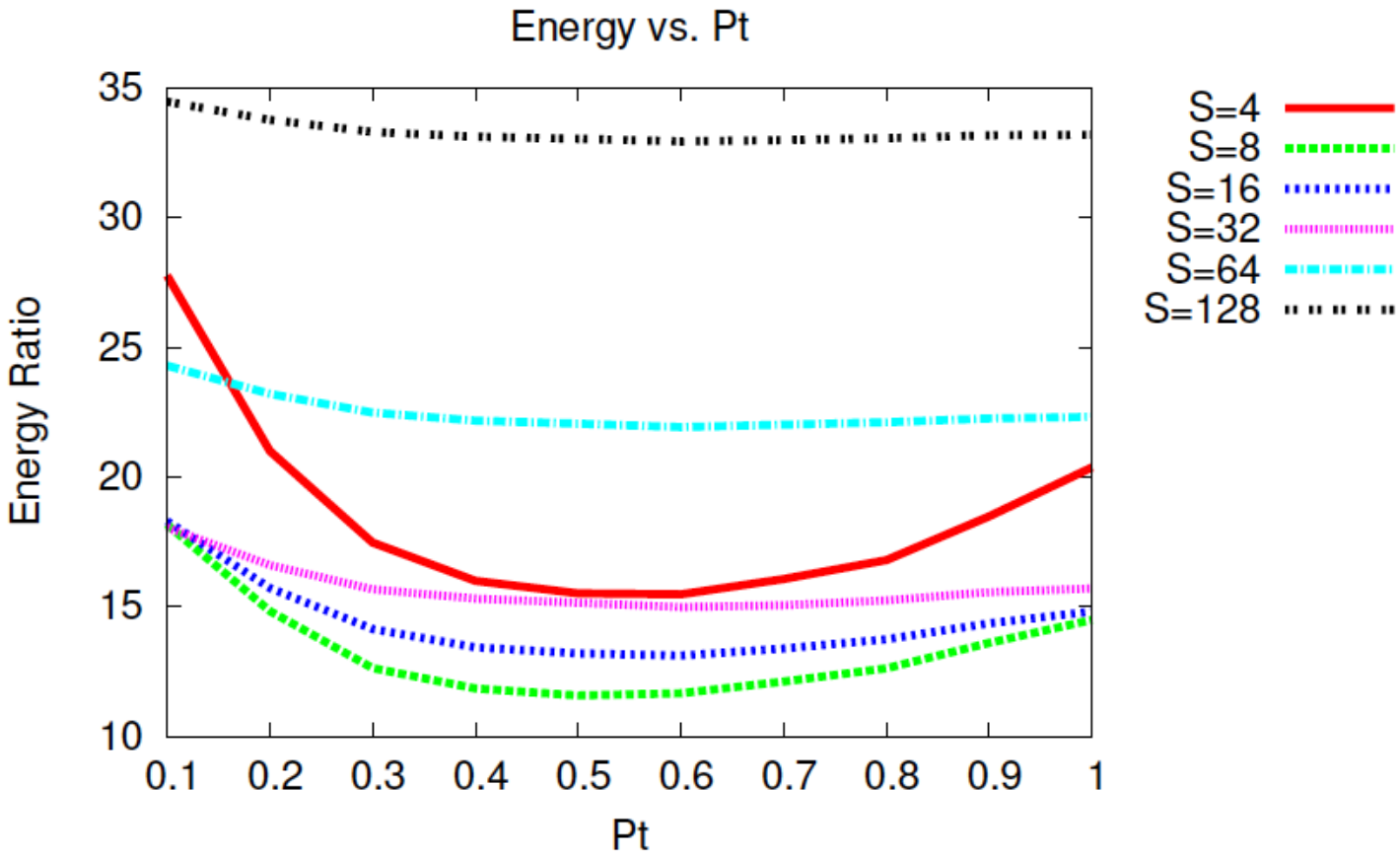




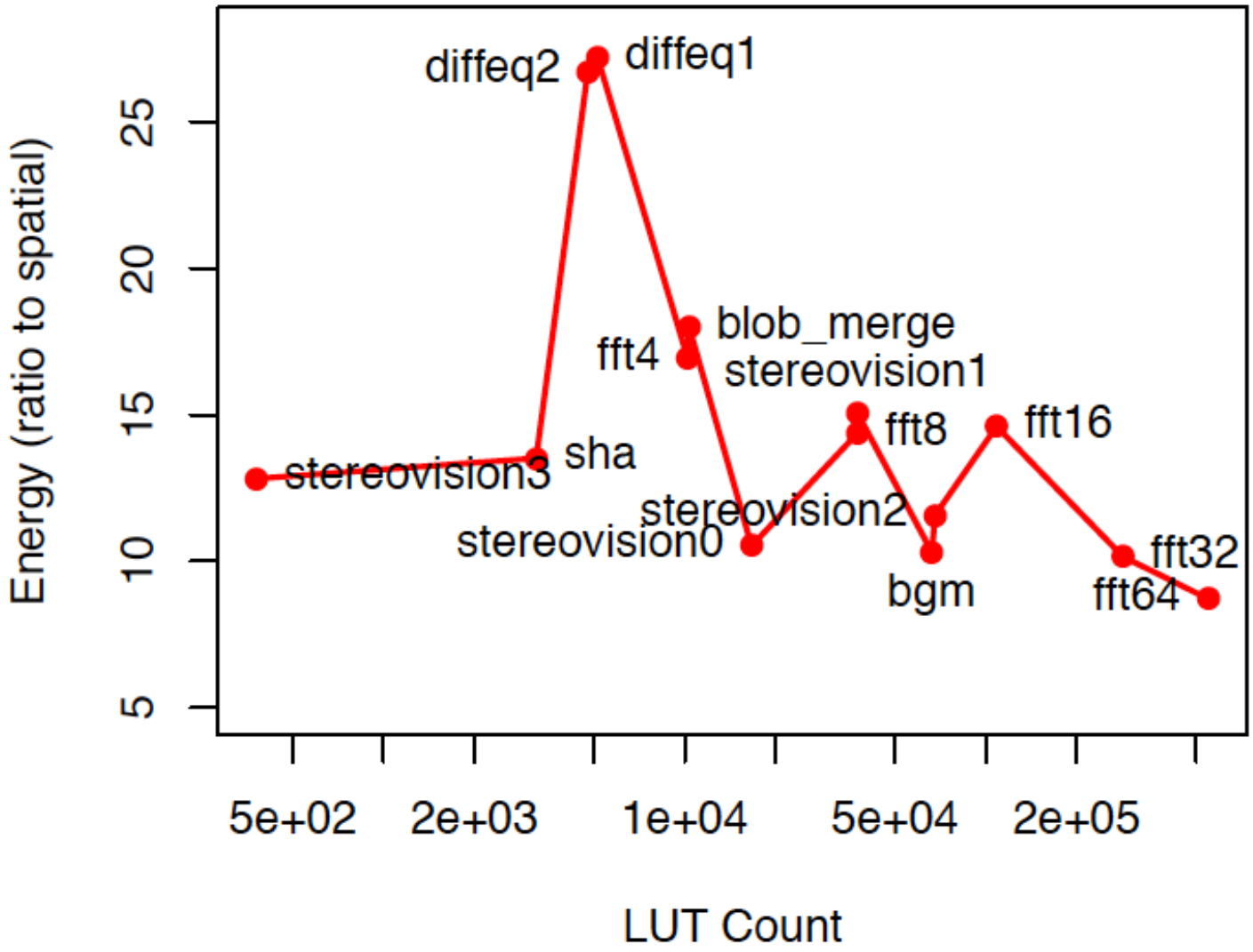
Space-Time Continuum



Energy in TS-Continuum (Ratio to Spatial)



All Benchmarks



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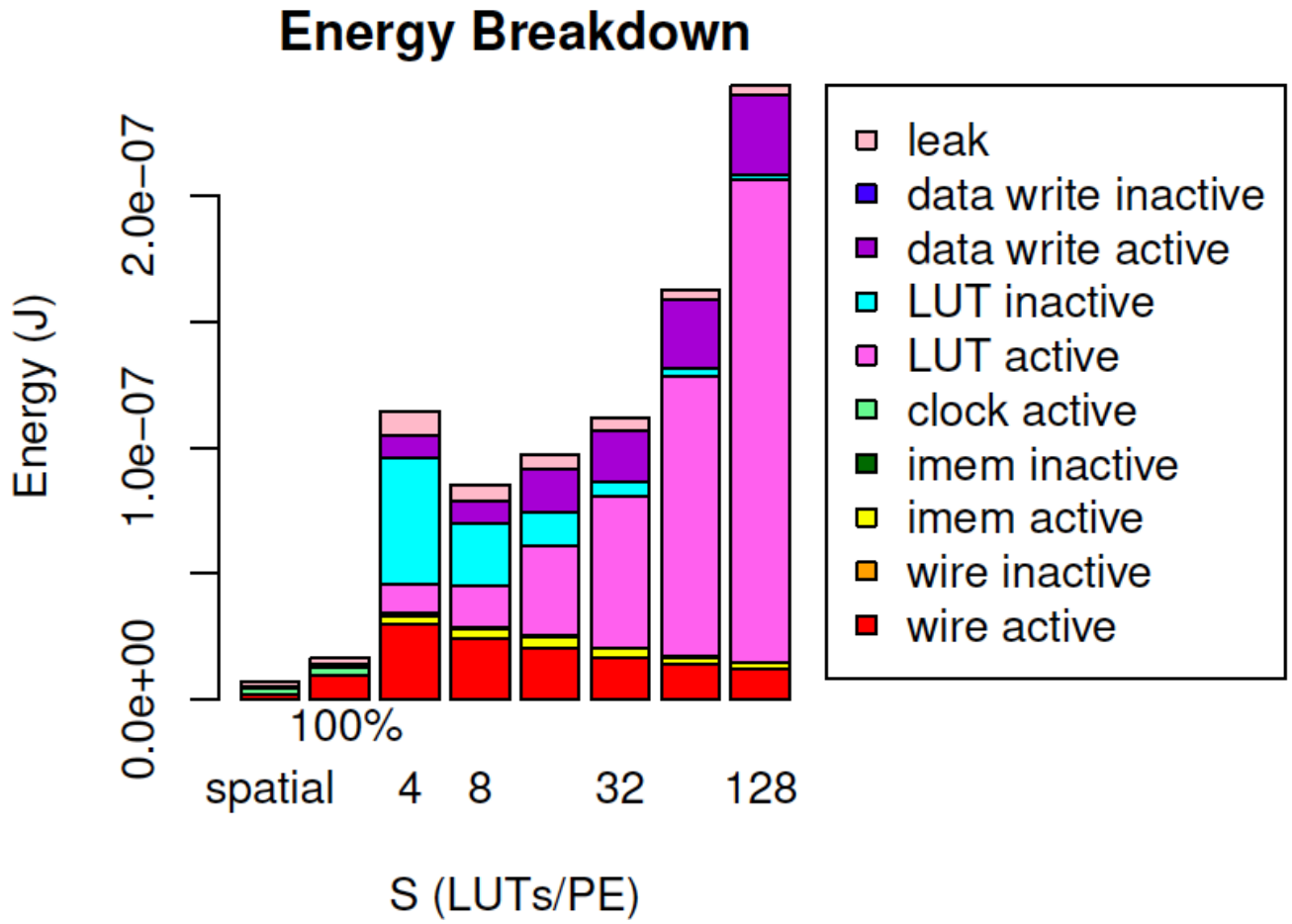
What Happened to Energy?



Energy Minimization Question

- Key issues
  - FPGAs long wires consume most energy
  - TM reduce area, reduce wire lengths
    - But add energy for memories and wire sharing
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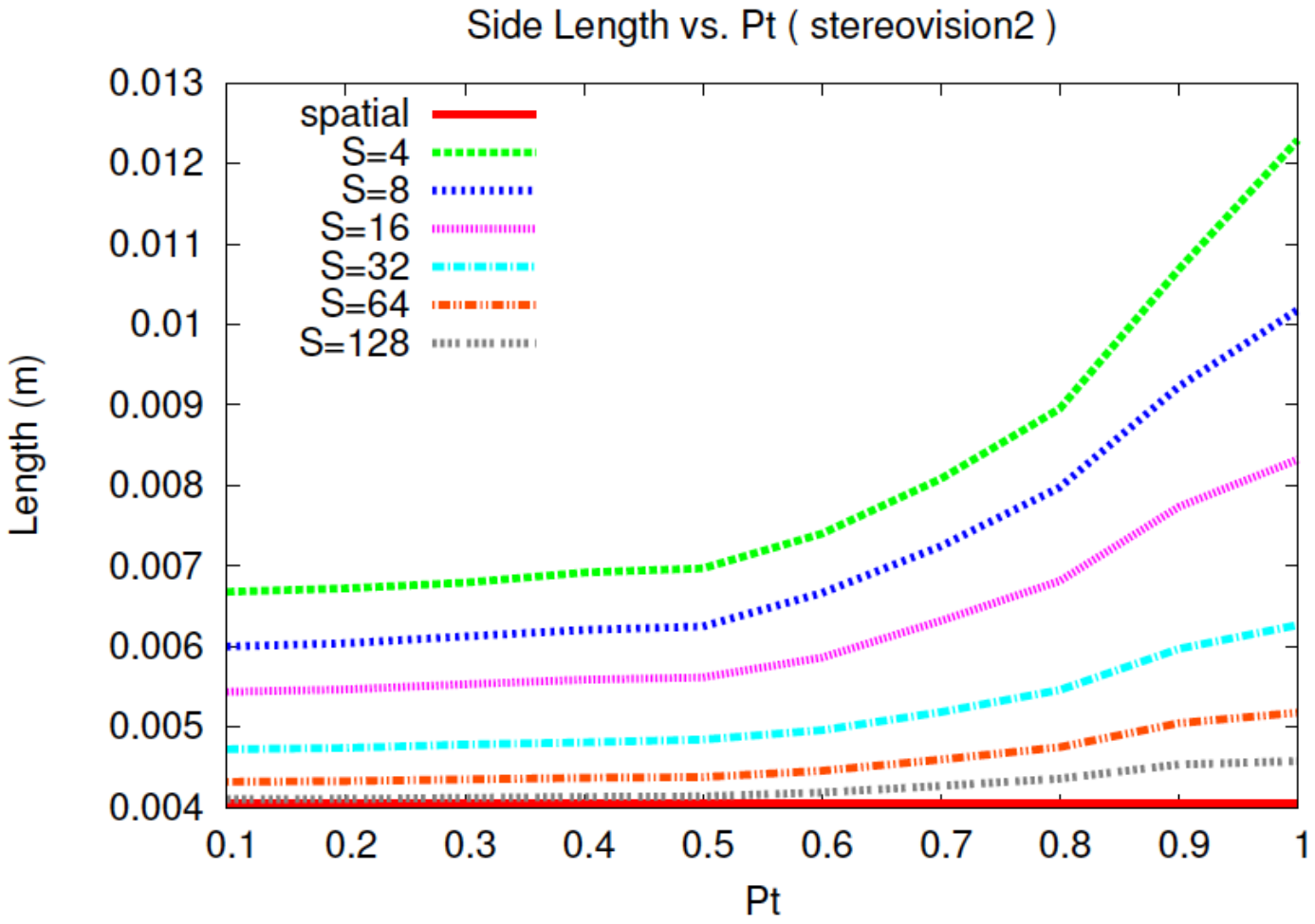
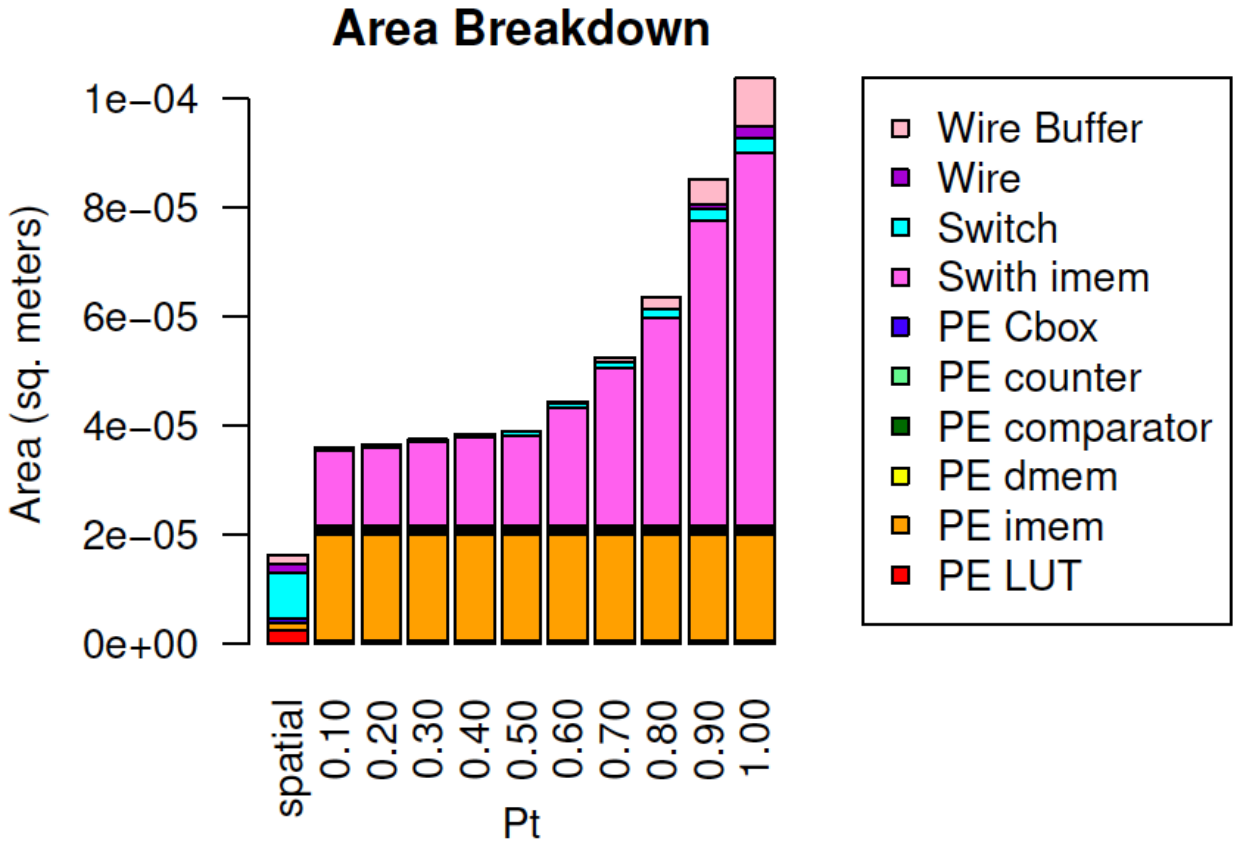
Wirelengths not Reduced

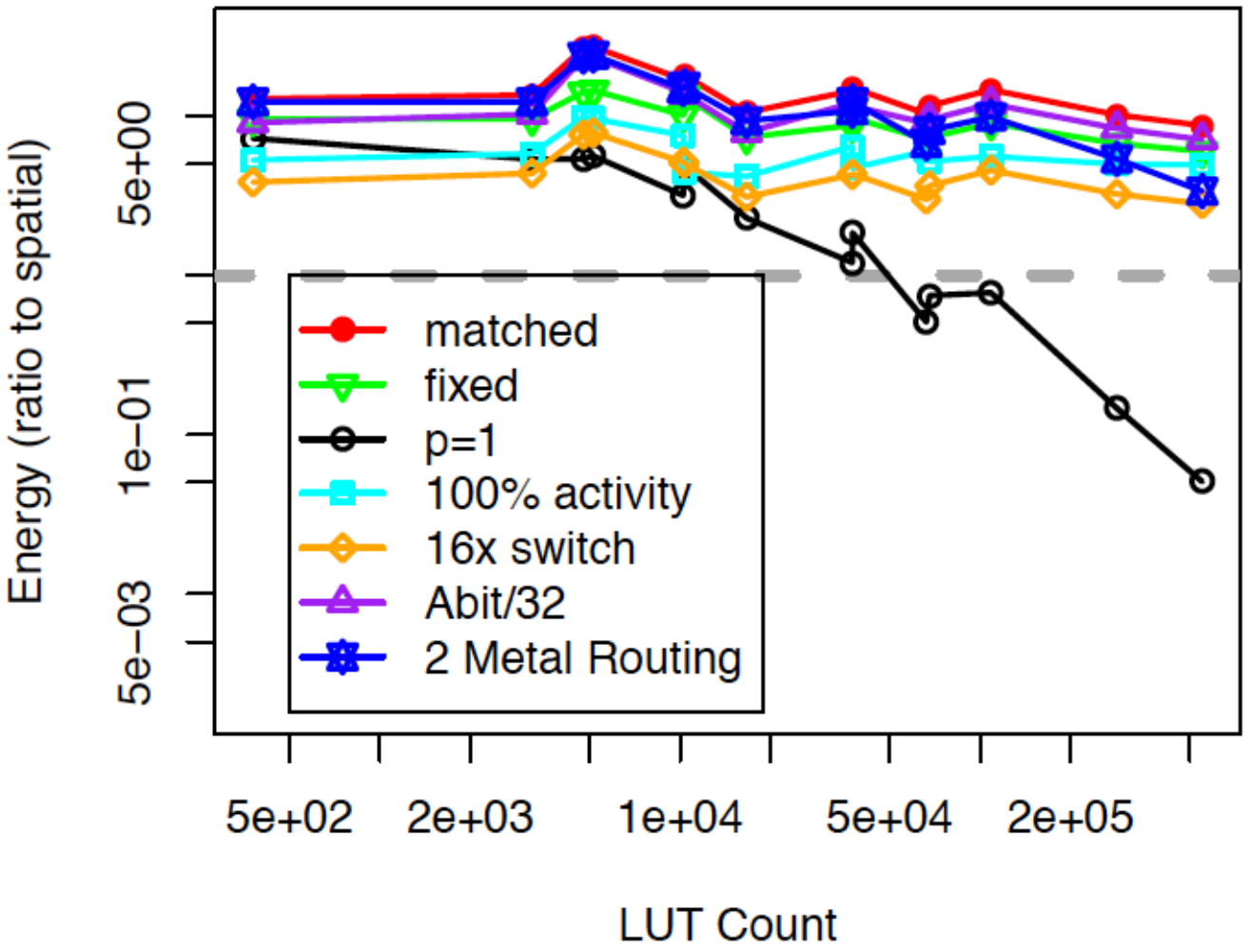


Why Wirelengths not Reduced?



- Wires don't dominate!

Sensitivity



Conclusion

- Spatial designs minimize energy
  - At least for typical interconnect requirements (Rent p < 0.75)
  - Up to half million LUTs
- Time-Multiplex designs can save area
  - When wire dominated → but typical designs are not **that** wire dominated
  - When switch dominated
    - But not enough to offset energy
      - Decorrelation
      - Added memory energy